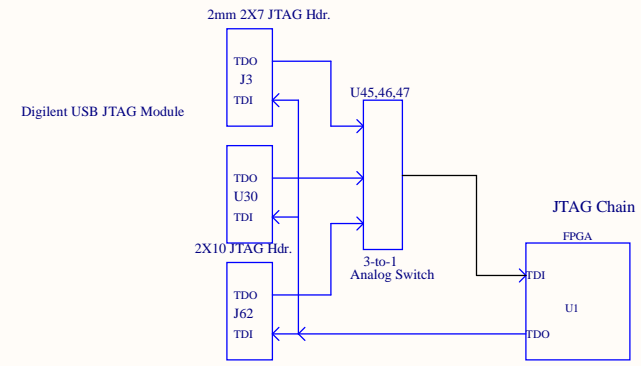
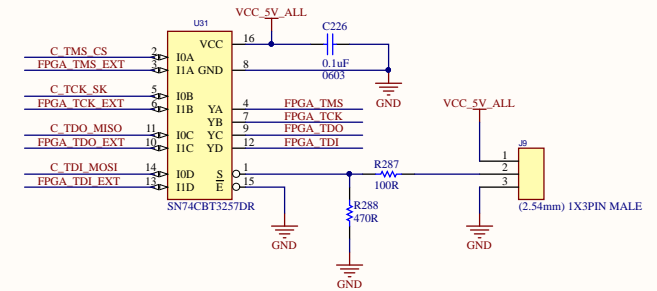
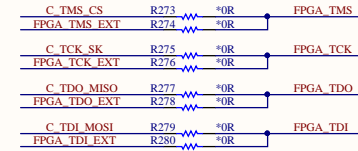
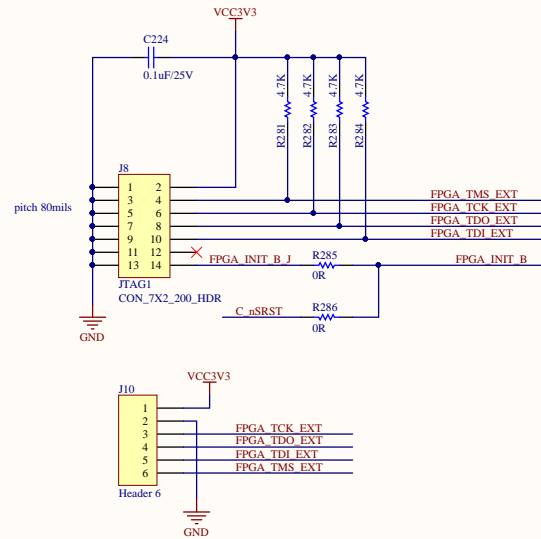
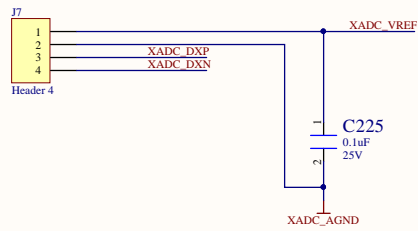
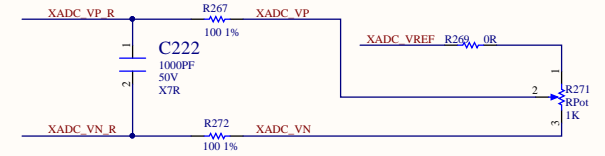
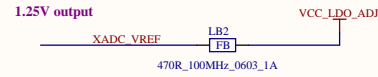
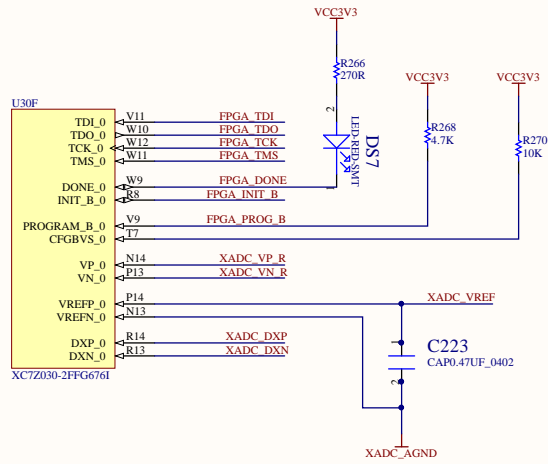


IIC Addressing	
0x110100	PCA9548
0x111101	SI570
0xxxxx00	FMC HPC
0xxxxx00	FMC LPC
0x101000	IIC EEPROM
0x010001	IIC Port Expander
0x011101	ADV7511
0x1100101	PMBUS Controller
0x101001	IIC RTC
0x1010000	SFP+
0x1101000	SI5324
0x1010000	DDR3 SODIMM

- 0 => EEPROM
- 1 => SI5324
- 2 => LPC
- 3 => HDMI
- 4 => SFP1
- 5 => SFP2
- 6 => WM8978
- 7 => ADJ CLOCK

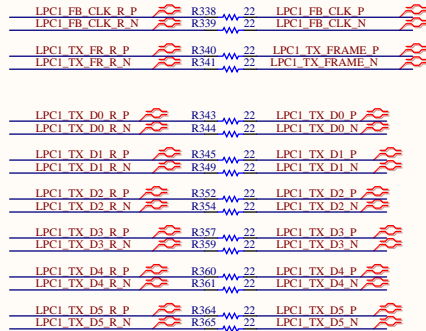
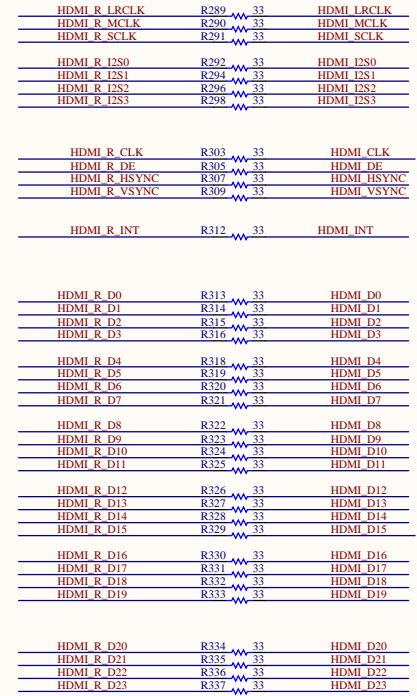
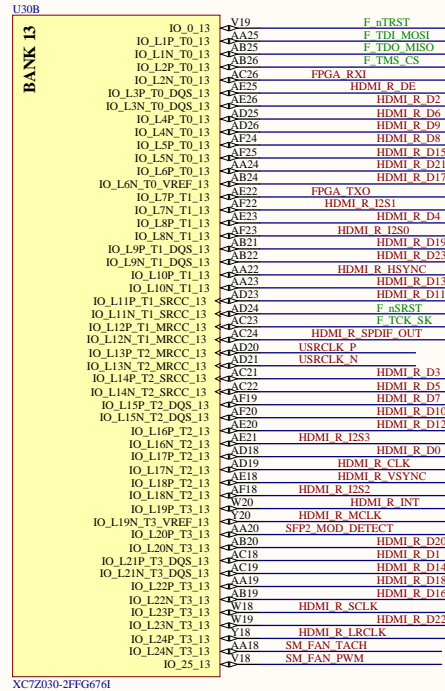
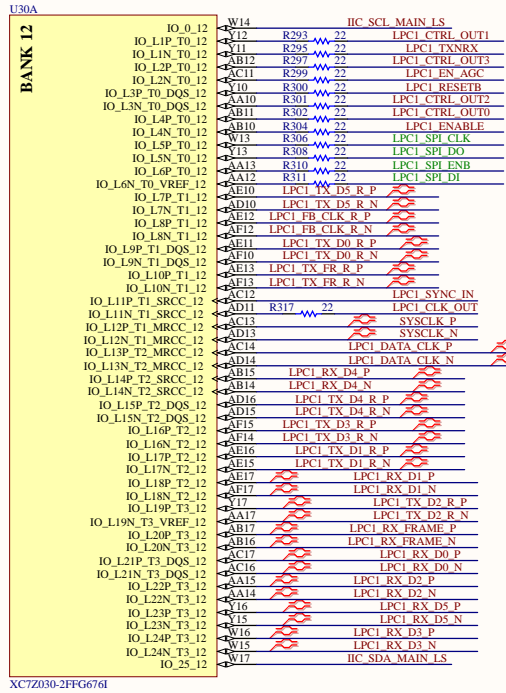




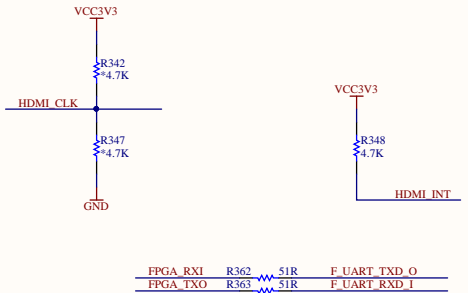
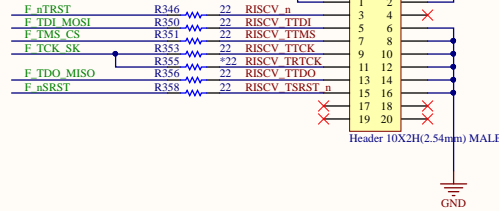
BANK12 VADJ_IV8_FPGA

BANK12-13 HR = High Range I/O with support for I/O voltage from 1.2V to 3.3V

BANK13 3.3V

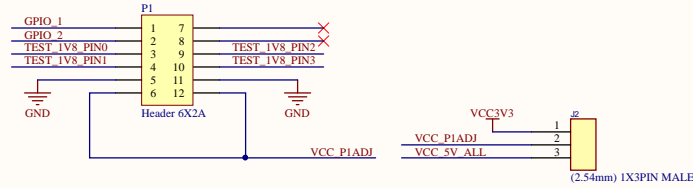
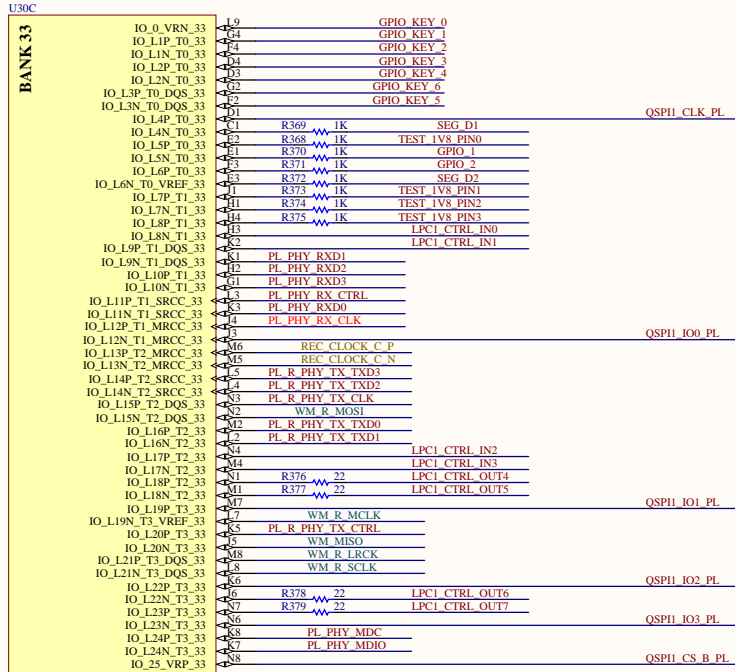


JTAG AS MASTER

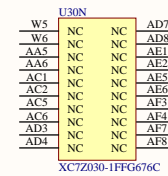
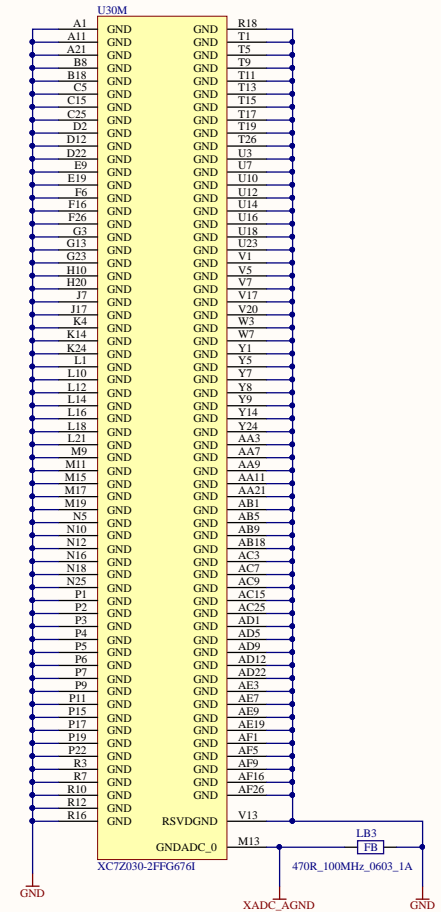
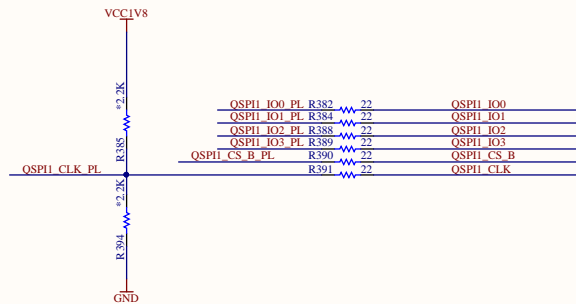
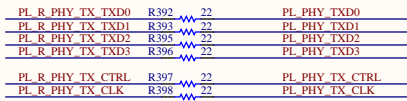


BANK 33,34,35 HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

BANK33 1.8V



XC7Z030-2FFG6761



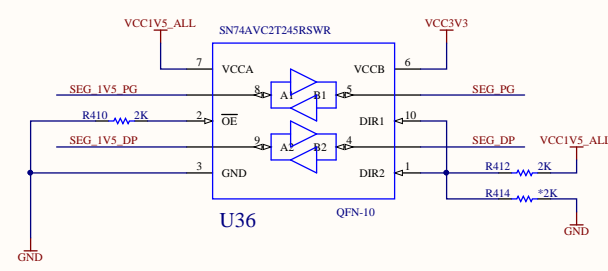
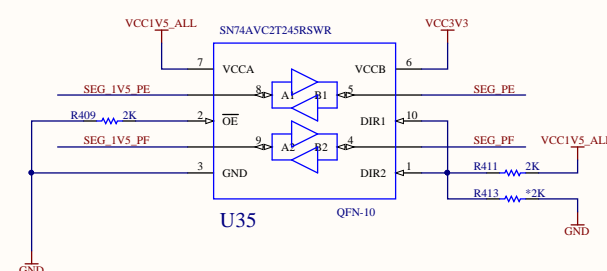
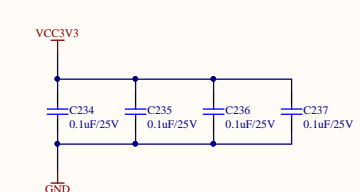
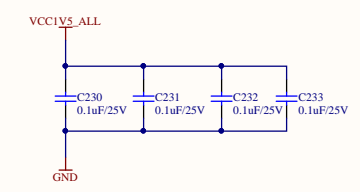
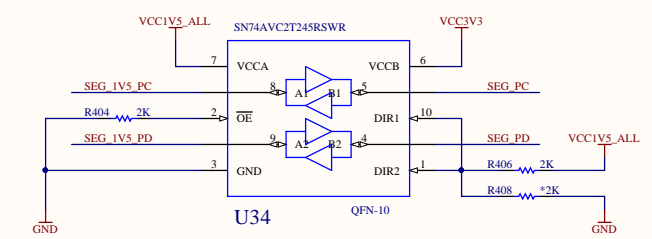
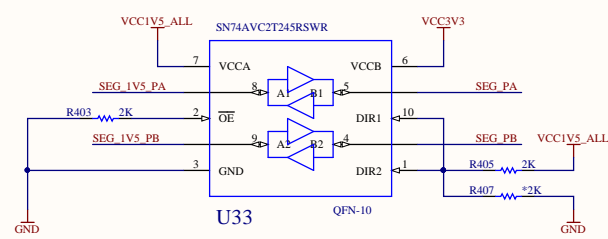
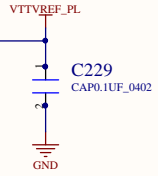
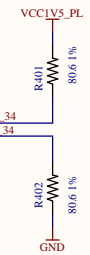
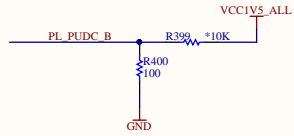
BANK 33,34,35 HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

BANK34 1.5V

U30D

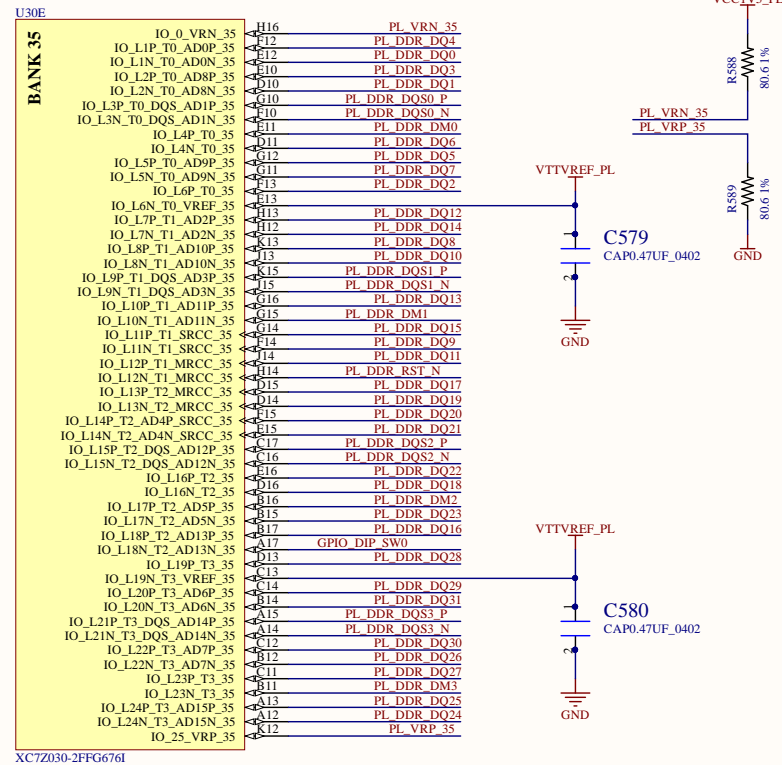
BANK 34		IO	PL	SEG
K11	PL_VRN_34	IO_0_VRN_34	VRN	SEG D6
H11		IO_L1P_T0_34		SEG D5
G6	PL_DDR_A8	IO_L1N_T0_34	DDR	
G5	PL_DDR_A9	IO_L2P_T0_34	DDR	
F9	PL_PUDC B	IO_L2N_T0_34	PUDC	
F9		IO_L3P_T0_DQS_34		
F9		IO_L3N_T0_DQS_34		
H6		IO_L4P_T0_34		
H6		IO_L4N_T0_34		
F10	SEG 1V5_PA	IO_L5P_T0_34		
F9	SEG 1V5_PB	IO_L5N_T0_34		
H8	PL_DDR_A13	IO_L6P_T0_34	DDR	
H8		IO_L6N_T0_VREF_34		
H5	PL_DDR_A6	IO_L7P_T1_34	DDR	
H5	PL_DDR_A11	IO_L7N_T1_34	DDR	
F9	PL_DDR_CKE_0	IO_L8P_T1_34	DDR	
H8	PL_DDR_WE_N	IO_L8N_T1_34	DDR	
F9	PL_DDR_A7	IO_L9P_T1_DQS_34	DDR	
F8		IO_L9N_T1_DQS_34		
F6	PL_DDR_A1	IO_L10P_T1_34	DDR	
F5	PL_DDR_A2	IO_L10N_T1_34	DDR	
F8	PL_DDR_A14	IO_L11P_T1_SRCC_34	DDR	
F7	PL_DDR_A0	IO_L11N_T1_SRCC_34	DDR	
F7	PL_DDR_A5	IO_L12P_T1_MRCC_34	DDR	
F7		IO_L12N_T1_MRCC_34		
F8	PL_DDR_CK_P	IO_L13P_T2_MRCC_34	DDR	
F7	PL_DDR_CK_N	IO_L13N_T2_MRCC_34	DDR	
F6		IO_L14P_T2_SRCC_34		
F6		IO_L14N_T2_SRCC_34		
F9	PL_DDR_RAS_N	IO_L15P_T2_DQS_34	DDR	
F9		IO_L15N_T2_DQS_34		
F10	SEG 1V5_DP	IO_L16P_T2_34		
A10	SEG 1V5_PG	IO_L16N_T2_34		
A9	SEG 1V5_PF	IO_L17P_T2_34		
A8	SEG 1V5_PE	IO_L17N_T2_34		
F7	SEG 1V5_PD	IO_L18P_T2_34		
A7	SEG 1V5_PC	IO_L18N_T2_34		
F4	PL_DDR_BA0	IO_L19P_T3_VREF_34	DDR	
F3	PL_DDR_BA1	IO_L20P_T3_34	DDR	
F5	PL_DDR_A15	IO_L20N_T3_34	DDR	
F4	PL_DDR_A3	IO_L21P_T3_DQS_34	DDR	
F4		IO_L21N_T3_DQS_34		
A4	PL_DDR_DOT0	IO_L22P_T3_34	DDR	
A3	PL_DDR_A10	IO_L22N_T3_34	DDR	
F2	PL_DDR_A12	IO_L23P_T3_34	DDR	
F1	PL_DDR_BA2	IO_L23N_T3_34	DDR	
F2	PL_DDR_A4	IO_L24P_T3_34	DDR	
A2	PL_DDR_CAS_N	IO_L24N_T3_34	DDR	
K10	PL_VRP_34	IO_25_VRP_34	VRP	

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BANK 33,34,35 HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

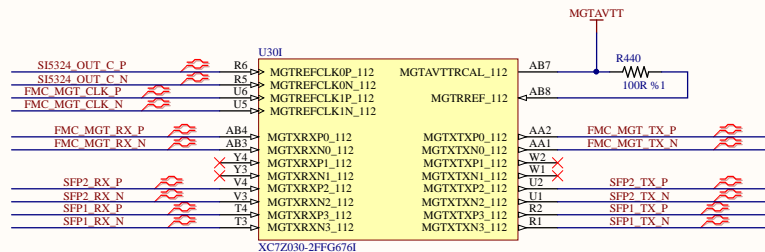
BANK35 1.5V



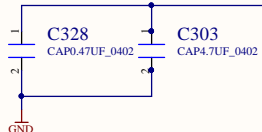
Company: FH	Title: FPGA_Bank35 of PE7030
Date: 2019-07-20 Time 3:46:05 PM	Engineer: WG RJ
Revision: V3	Sheet 6 of 42
	Size: B

BANK 33,34,35 HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.

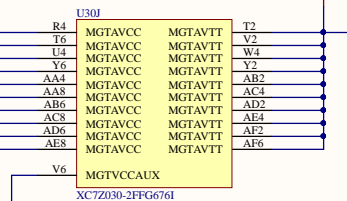
BANK500_112 CURRENT 1.8V



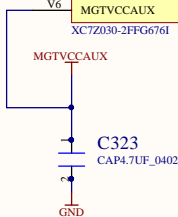
MGTAVCC



MGTAVCC



MGTAVCC



MGTAVTT



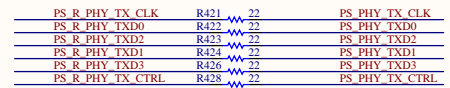
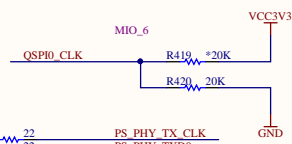
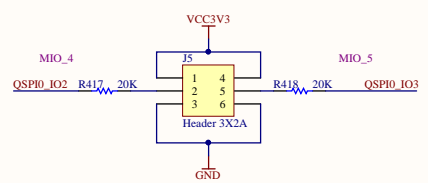
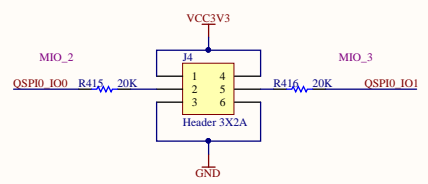
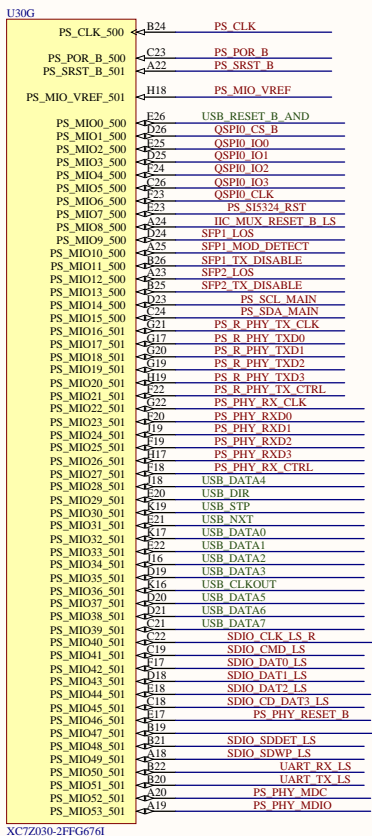
BANK500_501(1.8V-3.3V)

BANK500 3V3

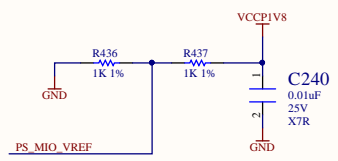
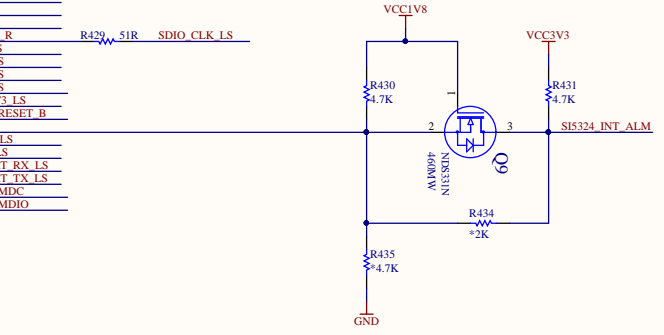
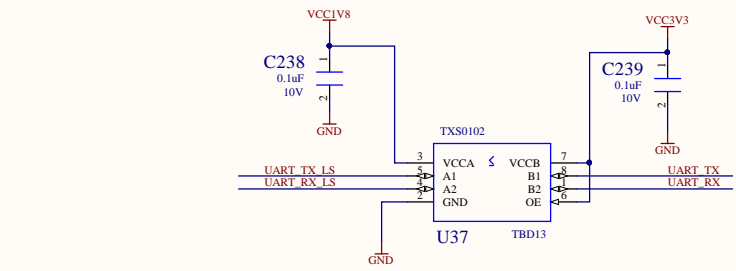
BANK501 1V8

BANK500 3V3

BANK501 1V8



MIO_5	MIO_4	MIO_3	JTAG
0	0	0	NOR_BOOT
0	0	1	NAND
0	1	0	QUAD_SPI
1	0	0	SD_CARD
1	1	0	



A

B

C

D

A

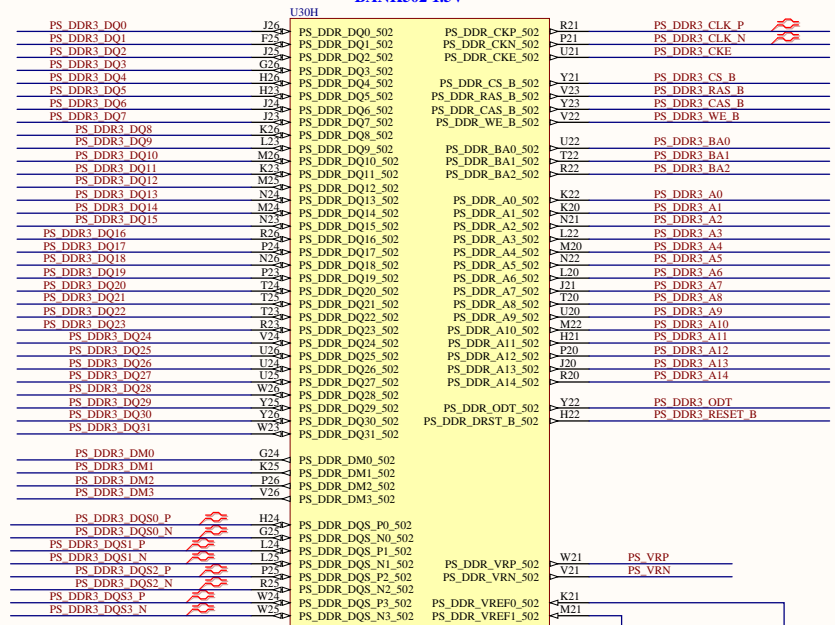
B

C

D

BANK502(1.2V-1.8V)

BANK502 1.5V



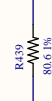
XC7Z030-2FFG6761

VCC1V5_PS



PS_VRN

PS_VRP



GND

VTTVREF_PS



C242
CAP0.47UF_0402

GND

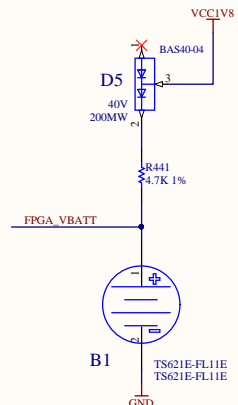
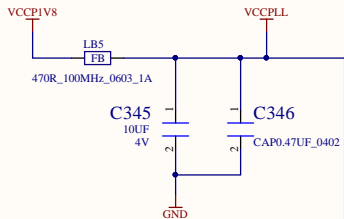
VTTVREF_PS



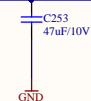
C241
CAP0.47UF_0402

GND

VCCINT



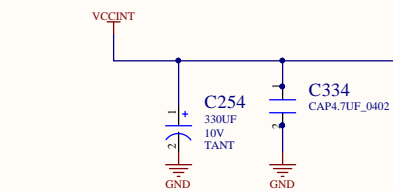
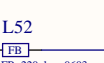
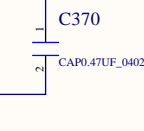
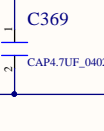
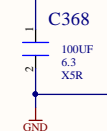
VCCAUX



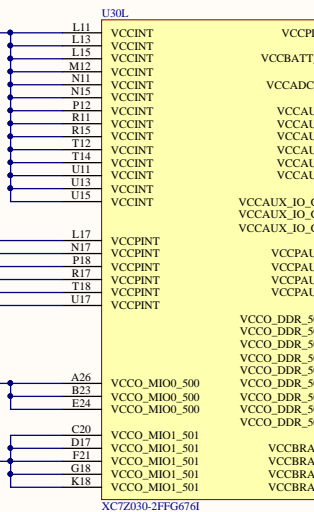
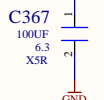
VCCAUX_IO



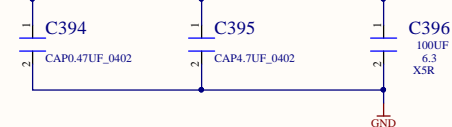
VCCPAUX



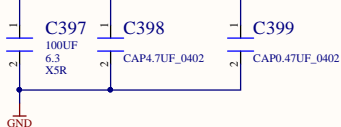
VCCPINT



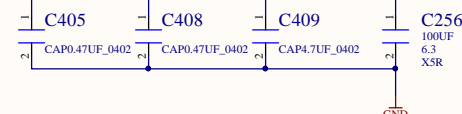
VCC_MIO0

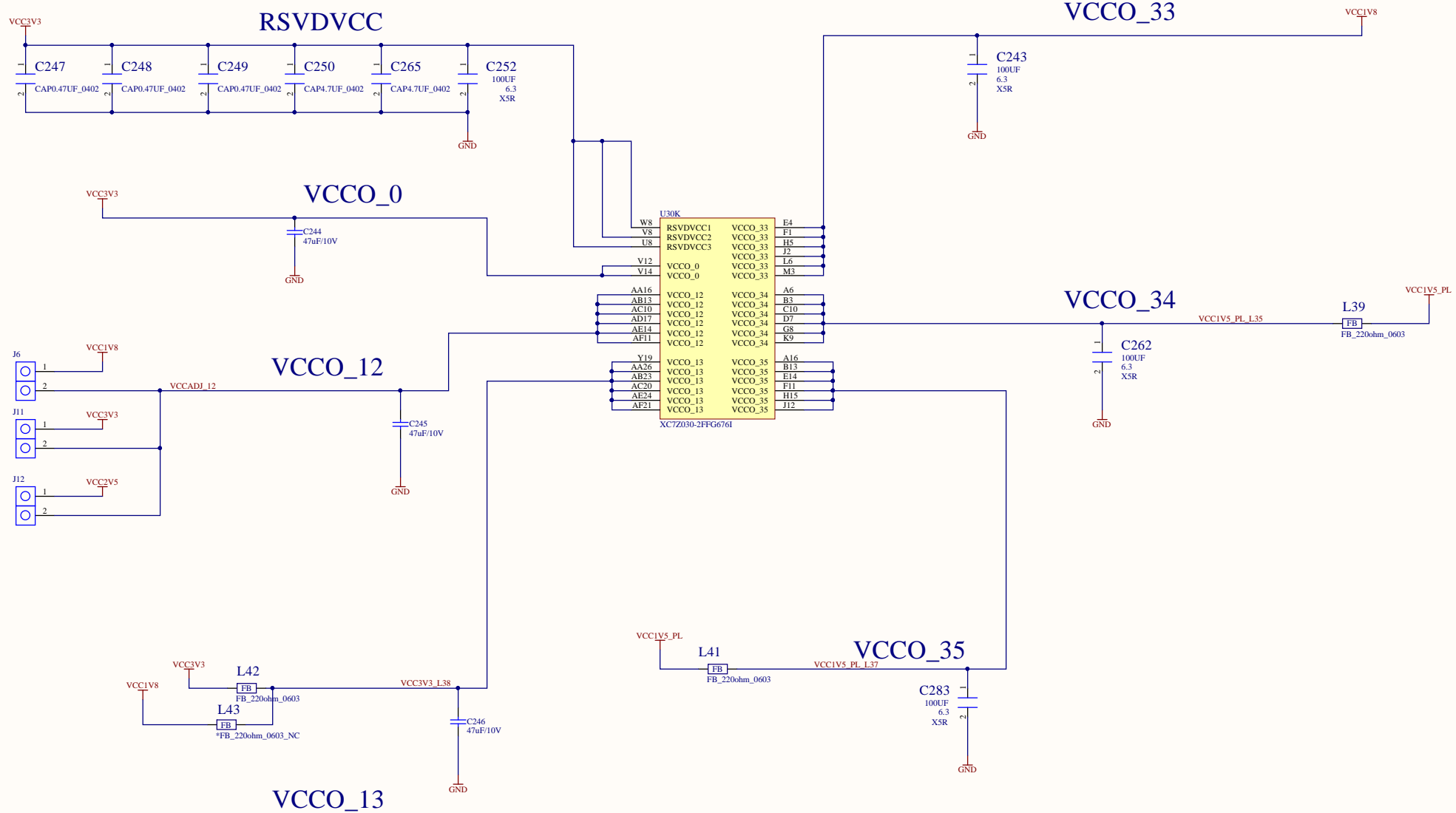


VCC_MIO1

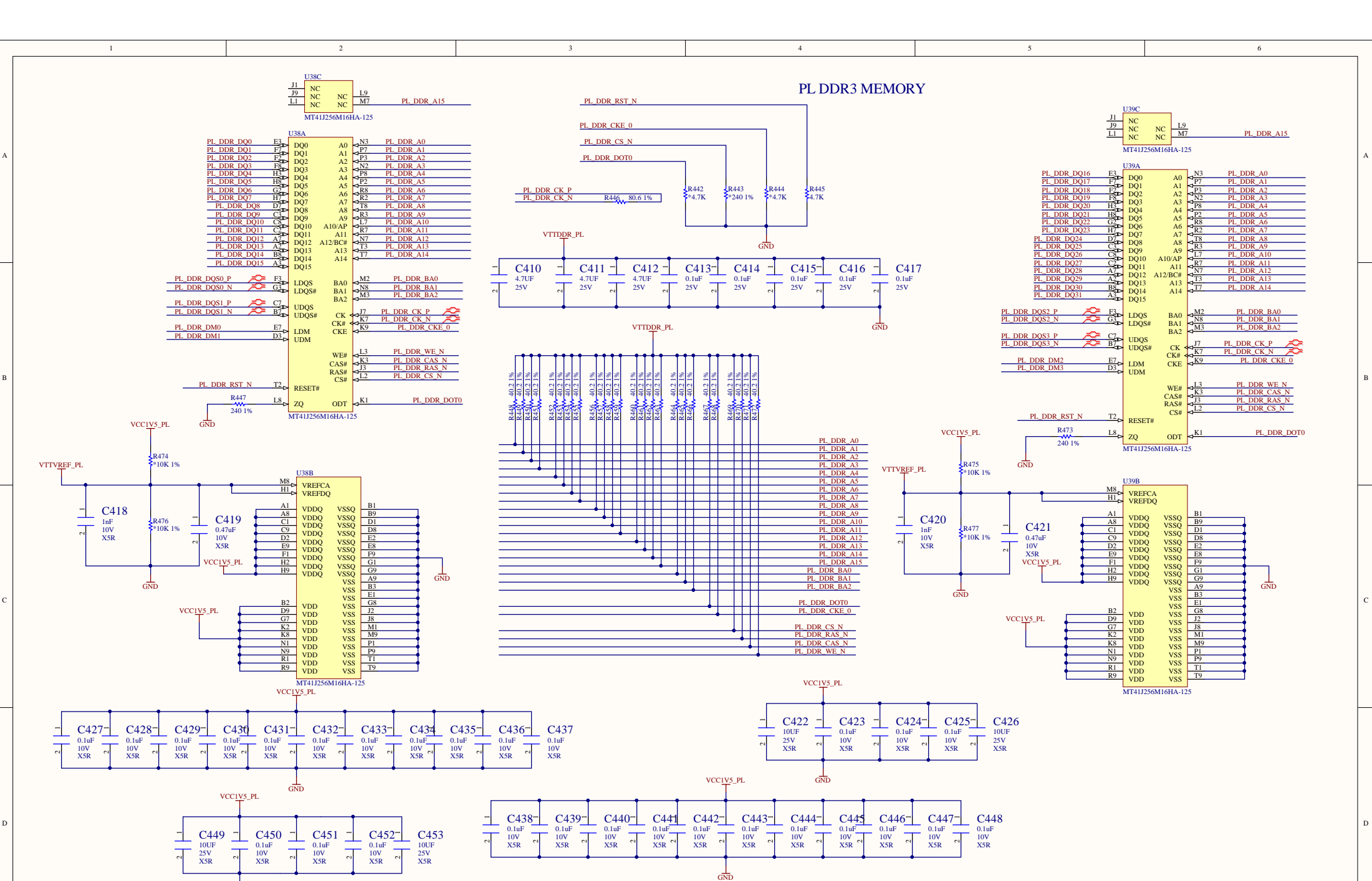


VCCBRAM

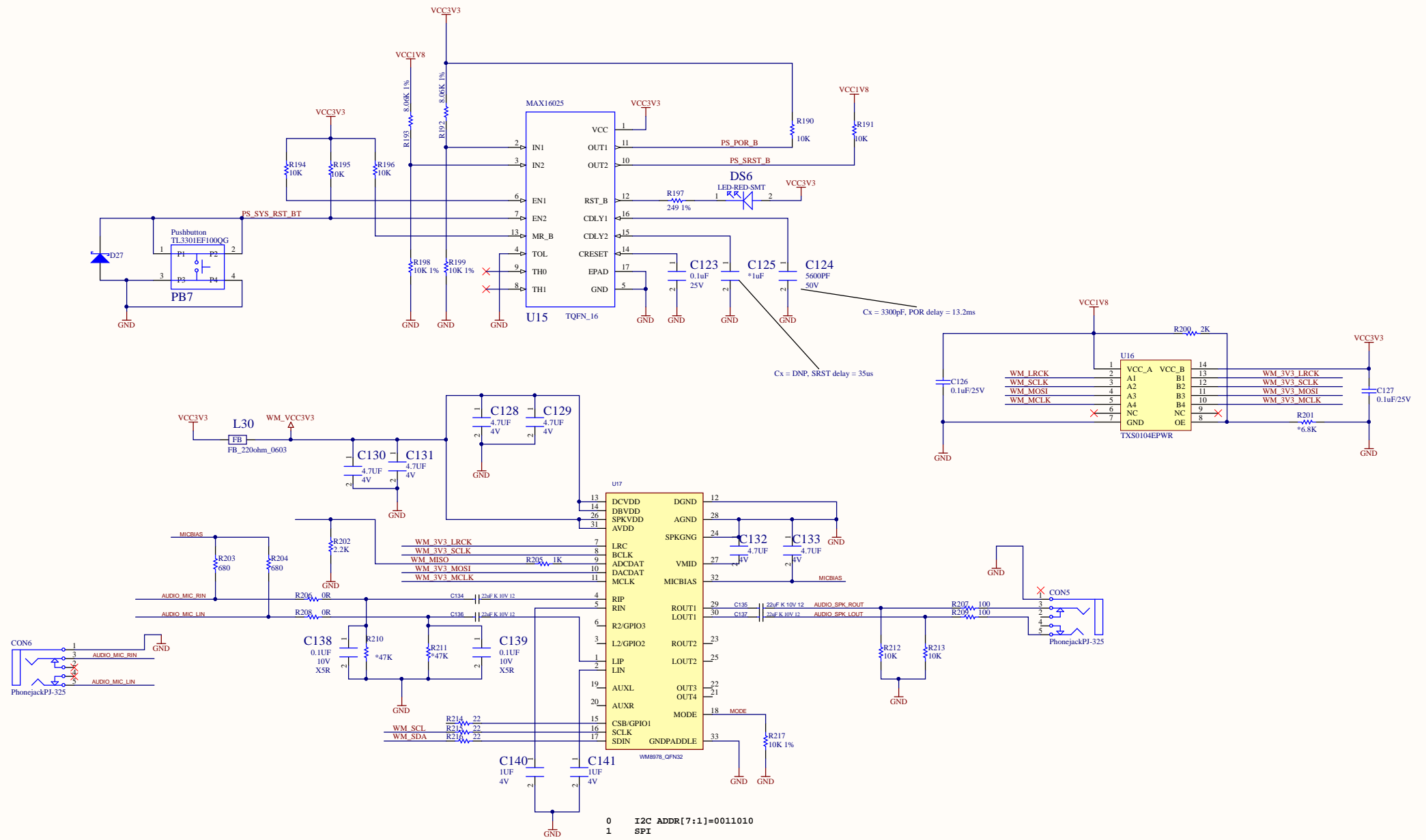


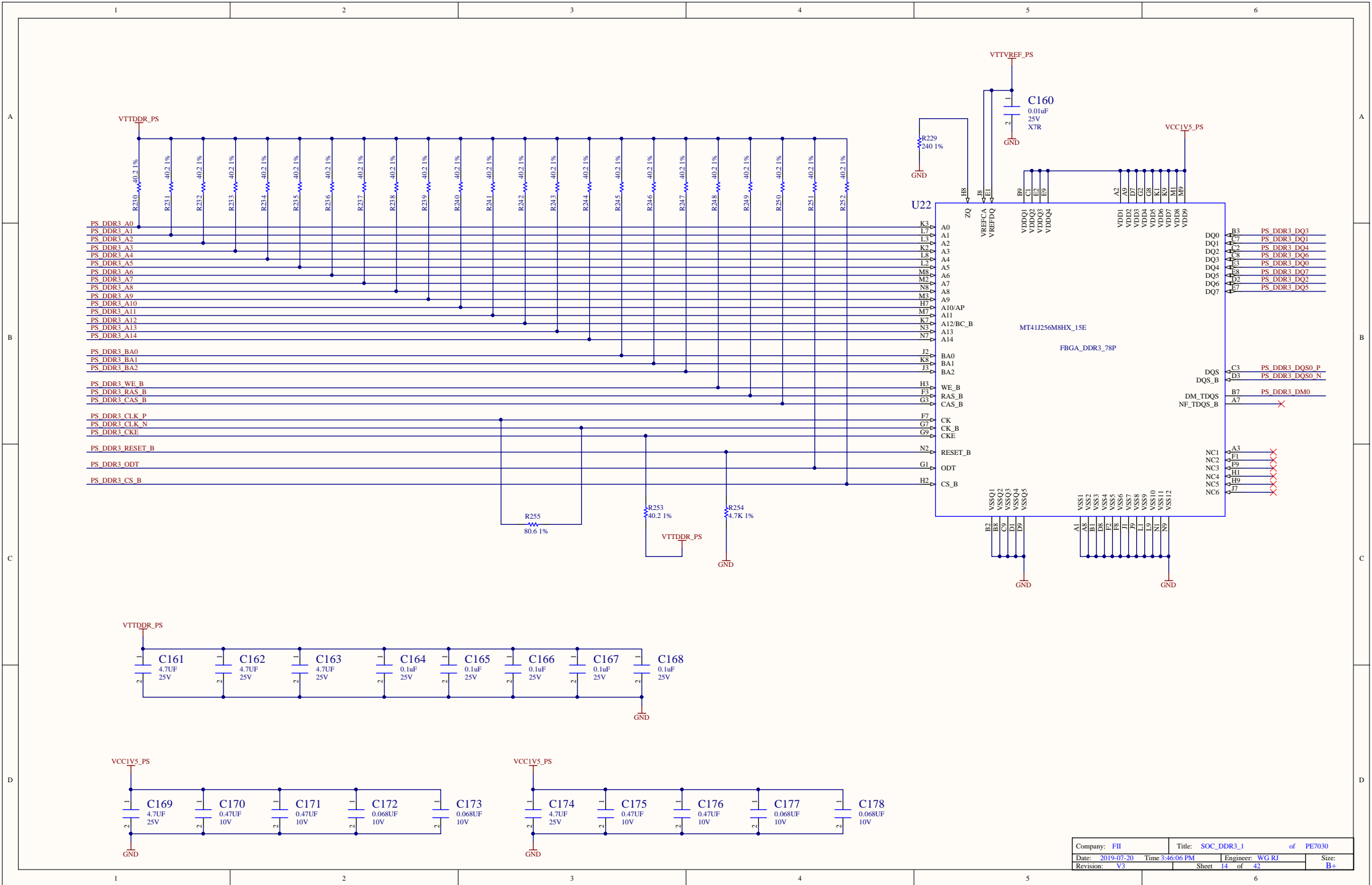


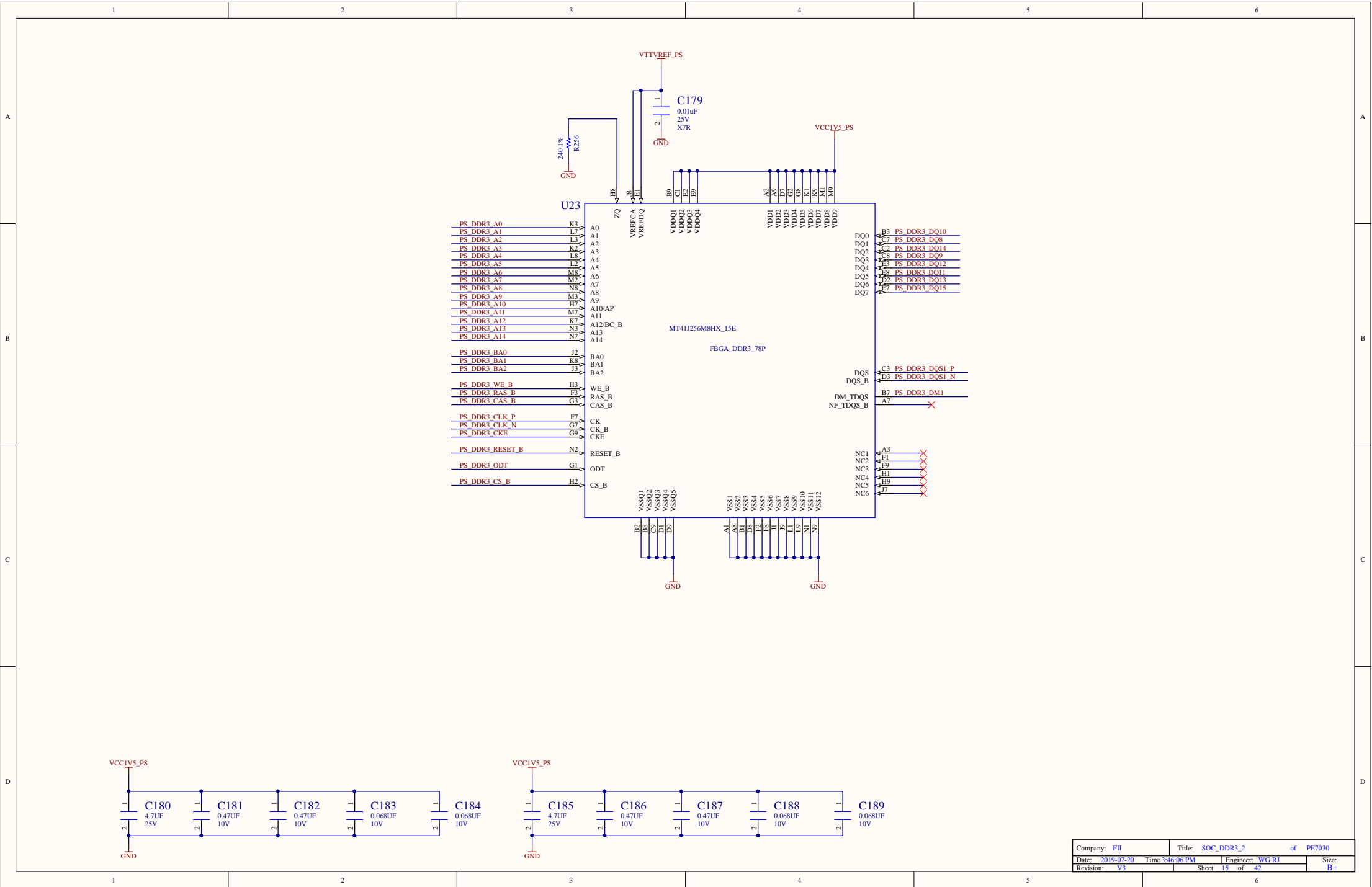
PL DDR3 MEMORY

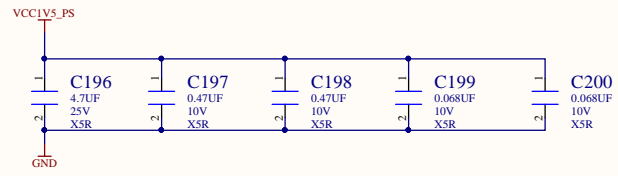
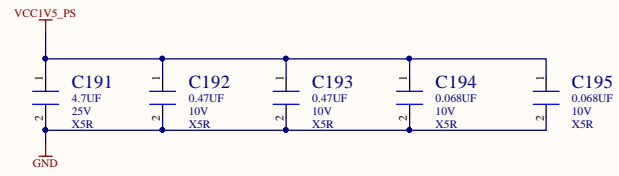
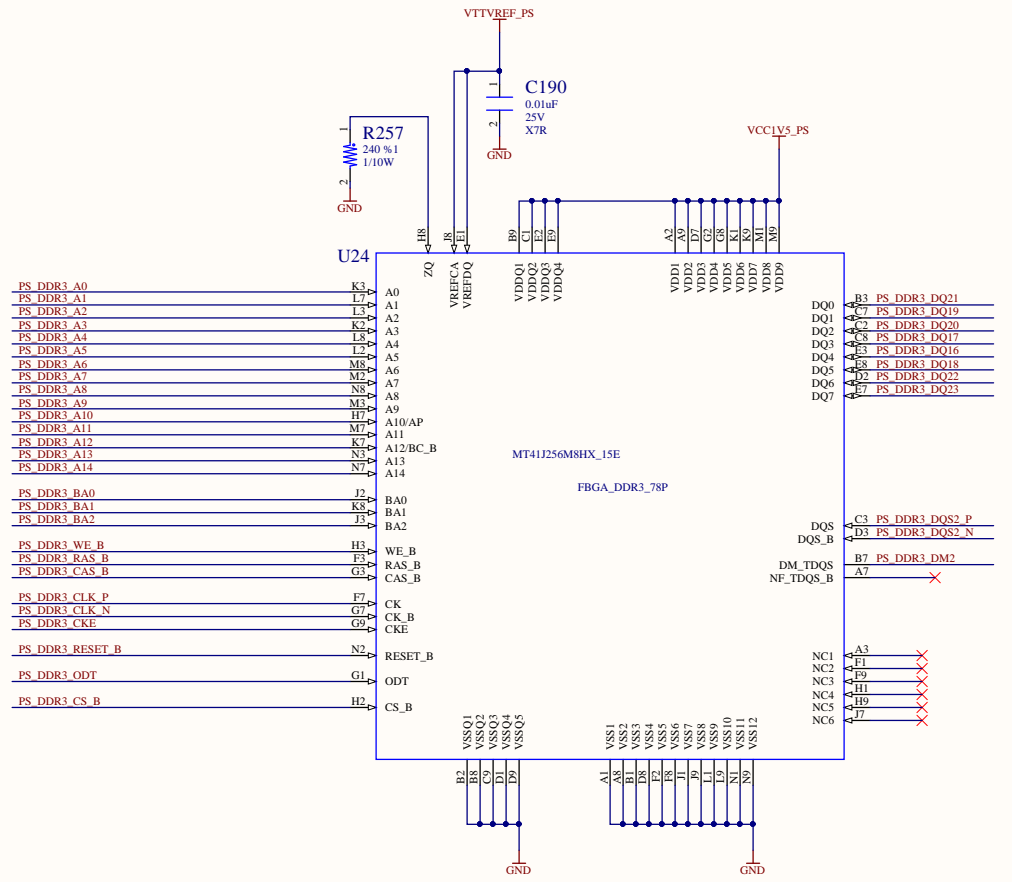


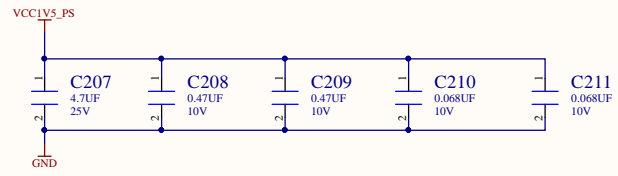
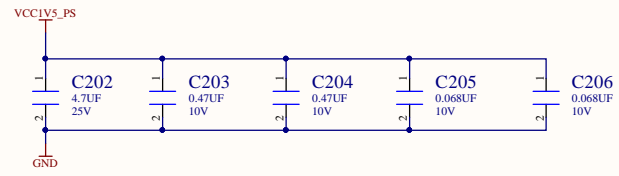
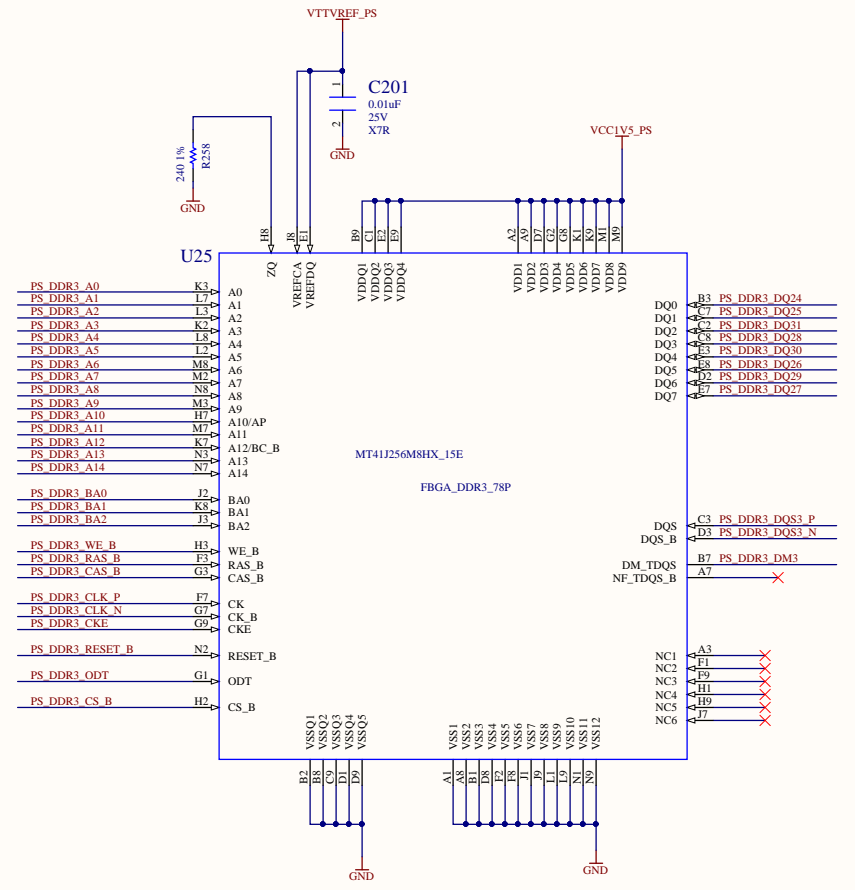
POR_B AND SRST_B



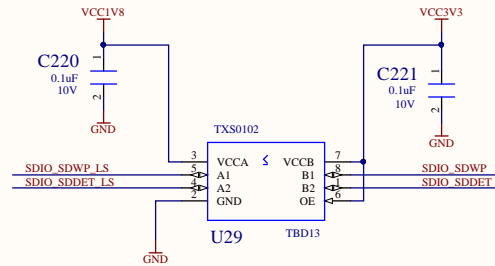
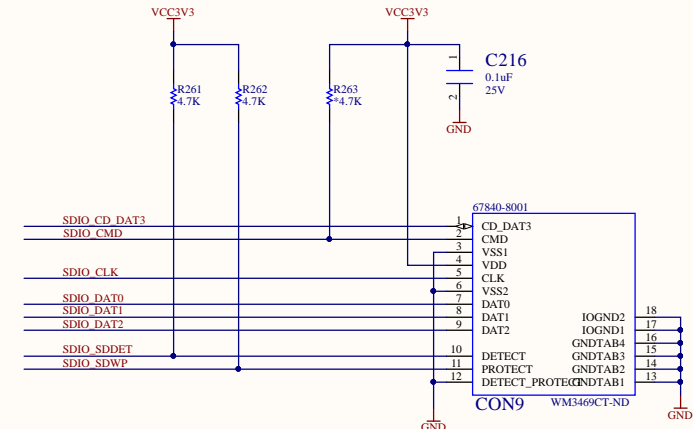
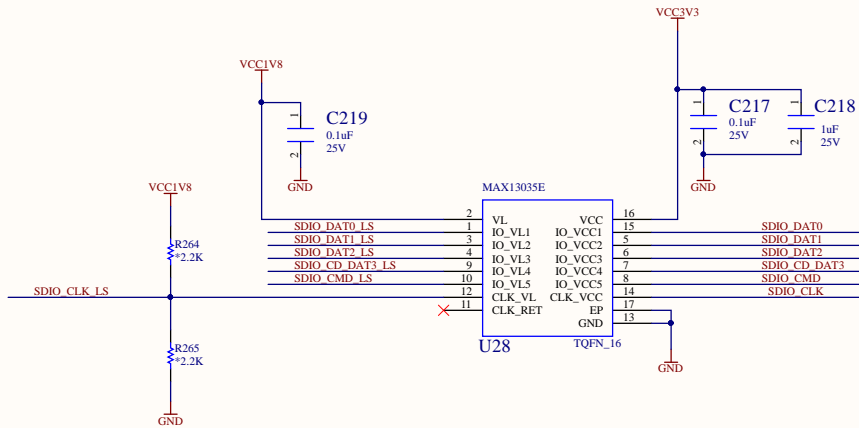
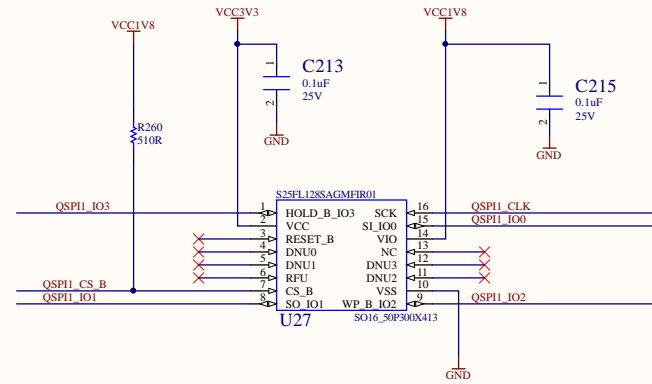
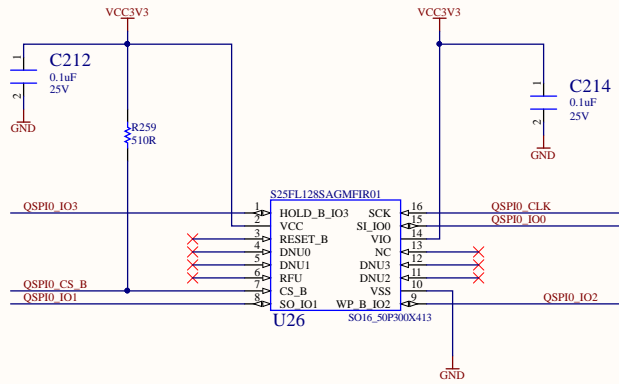


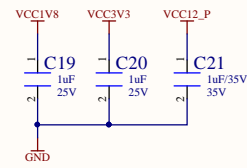
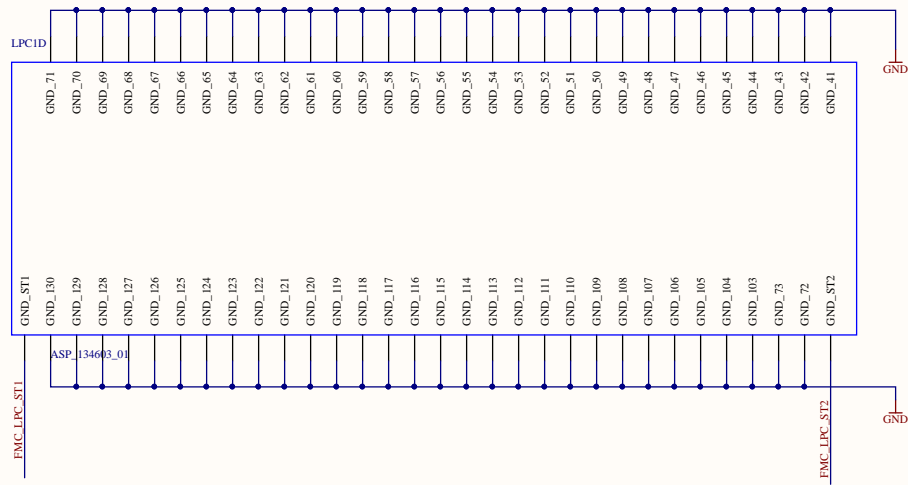
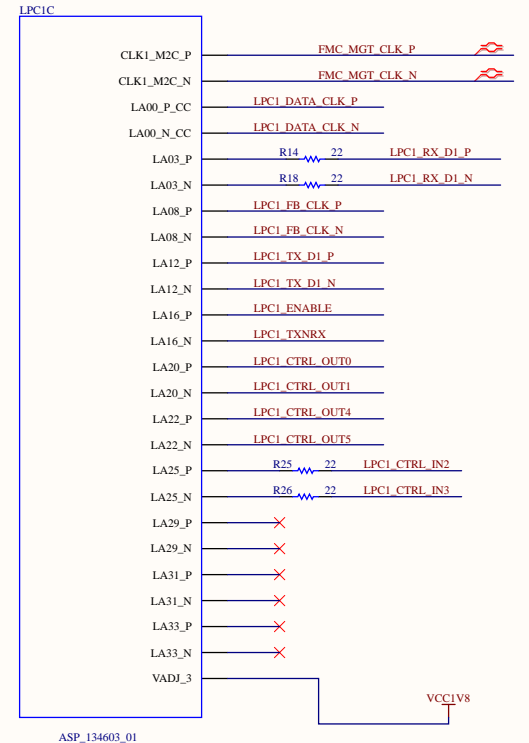
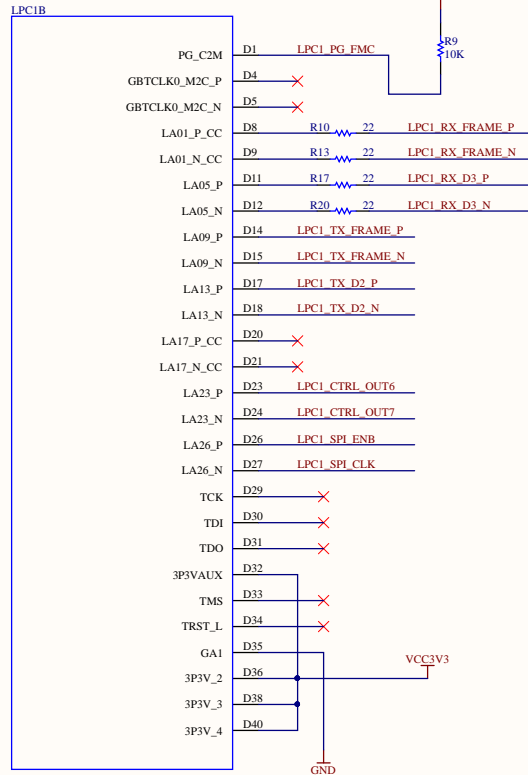
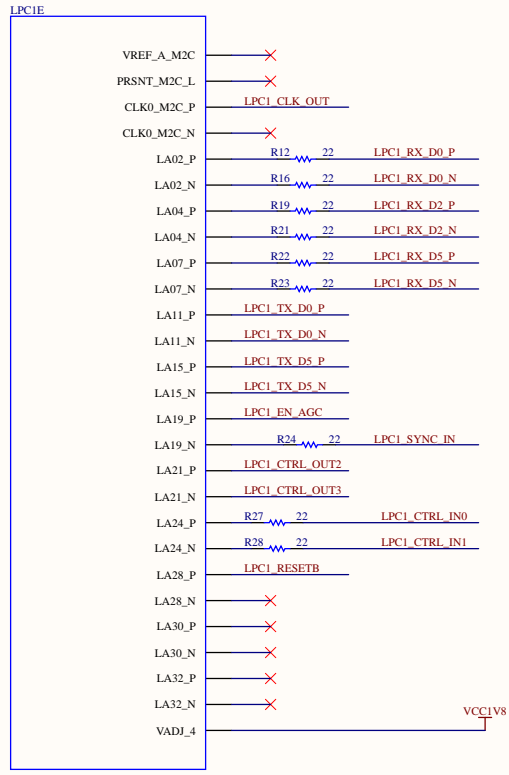
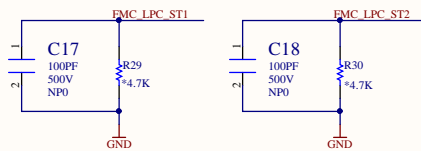
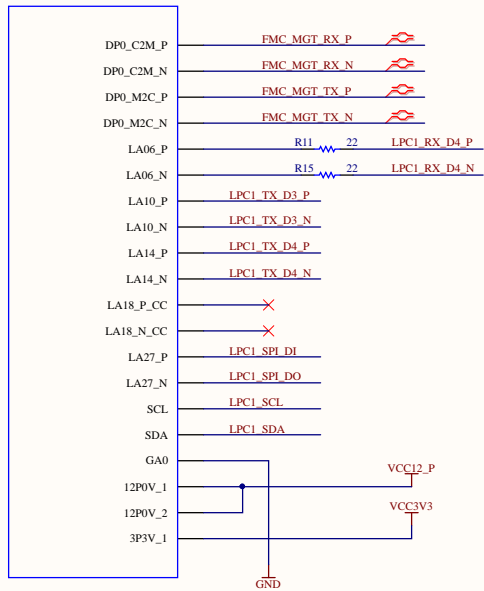






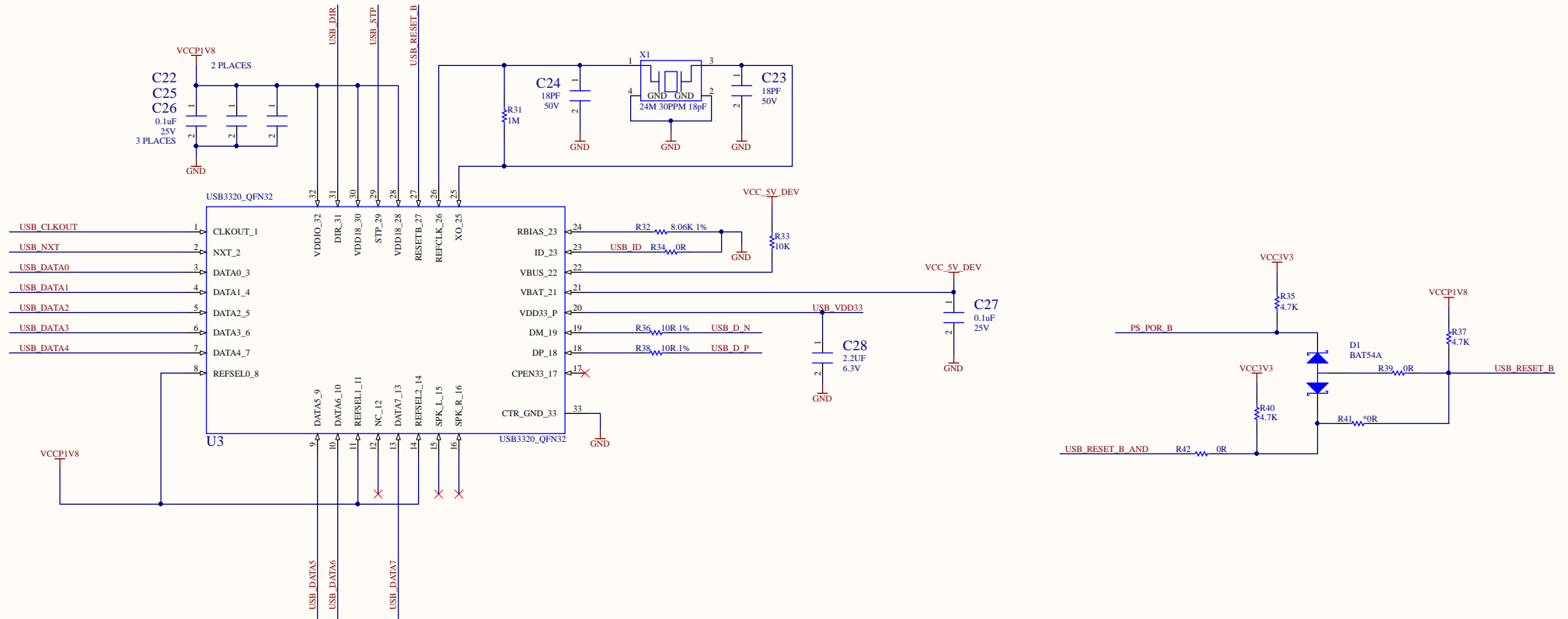
Dual Quad SPIs

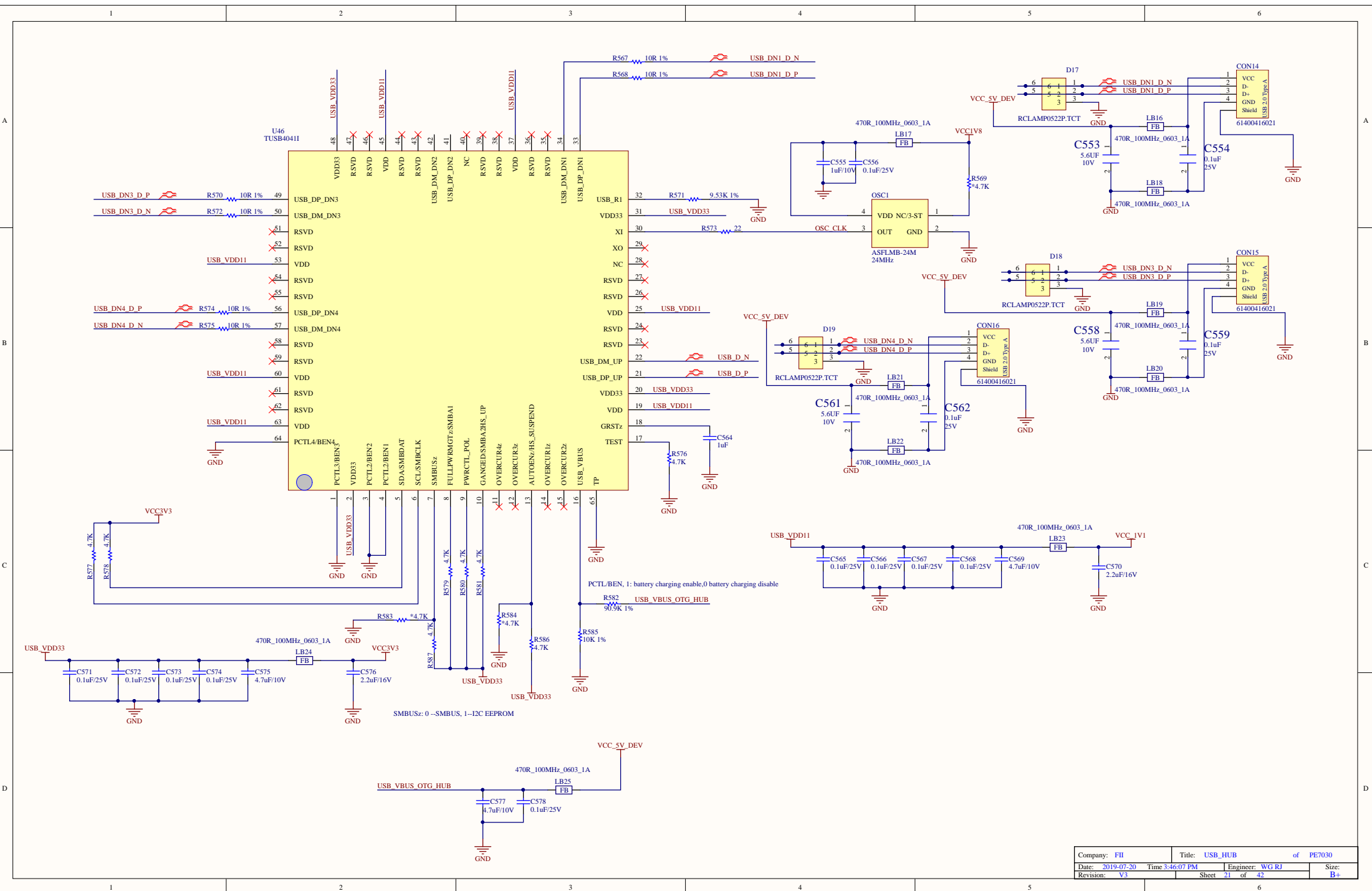




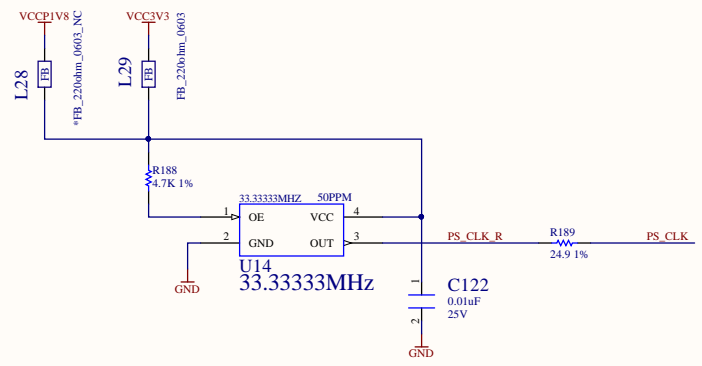
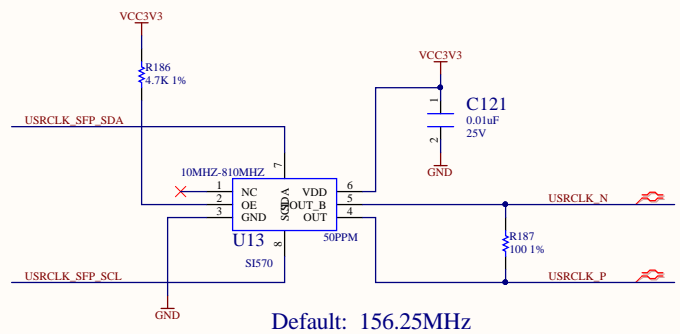
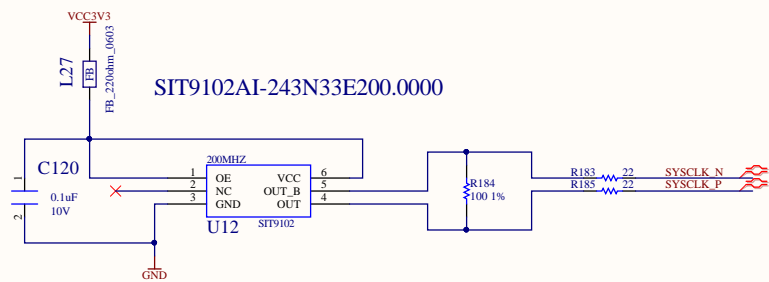
Company: FII	Title: FMC_LPC1	of PE7030
Date: 2019-07-20	Time 3:46:06 PM	Engineer: WG RJ
Revision: V3	Sheet 19	of 42
		Size: B+

USB 2.0 ULPI TRANSCEIVER AND CONNECTOR

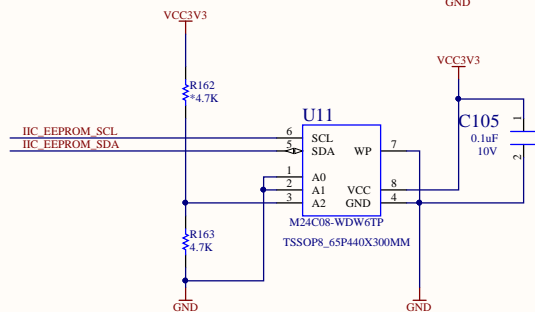
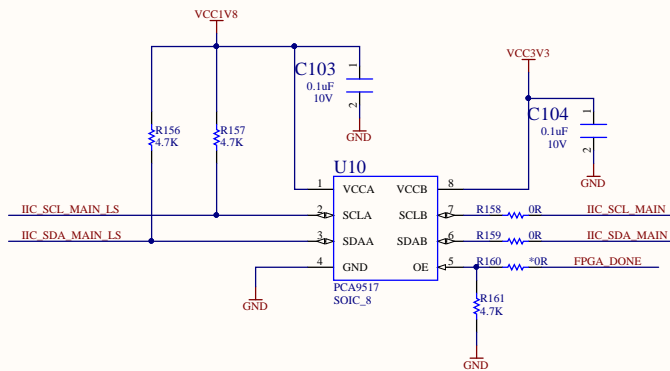
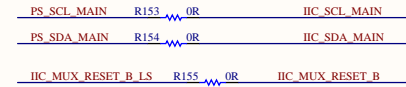
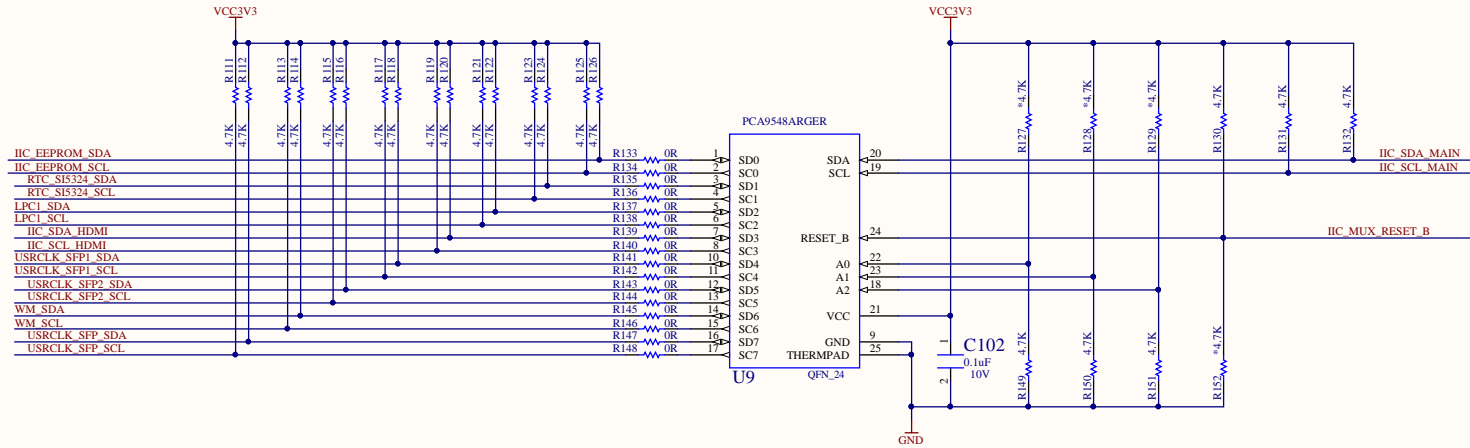


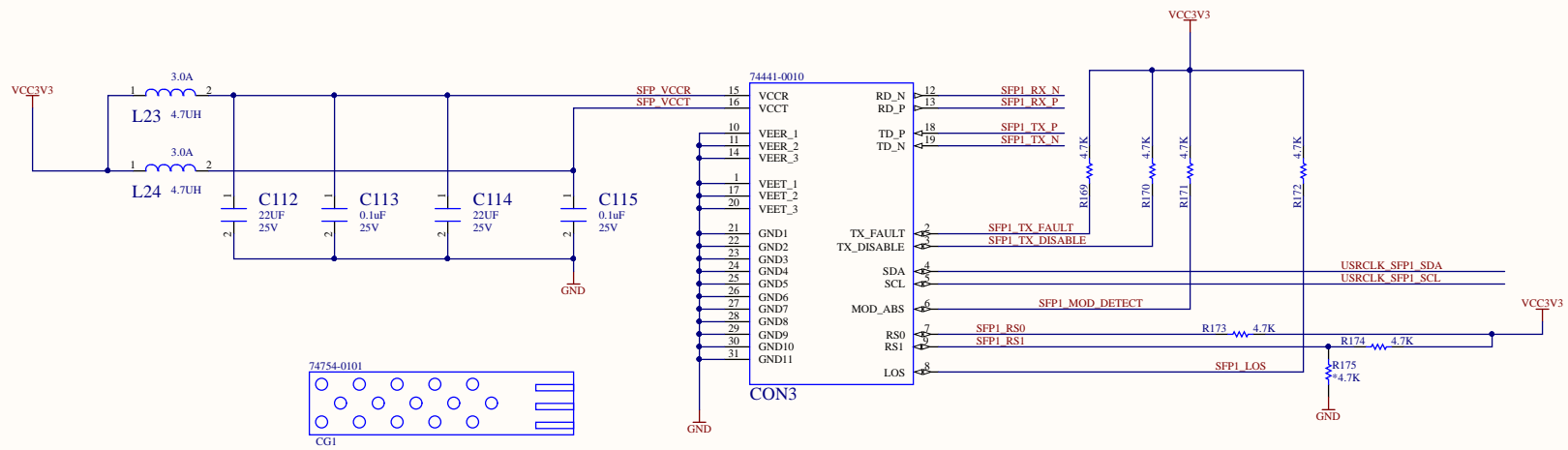


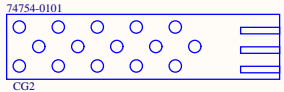
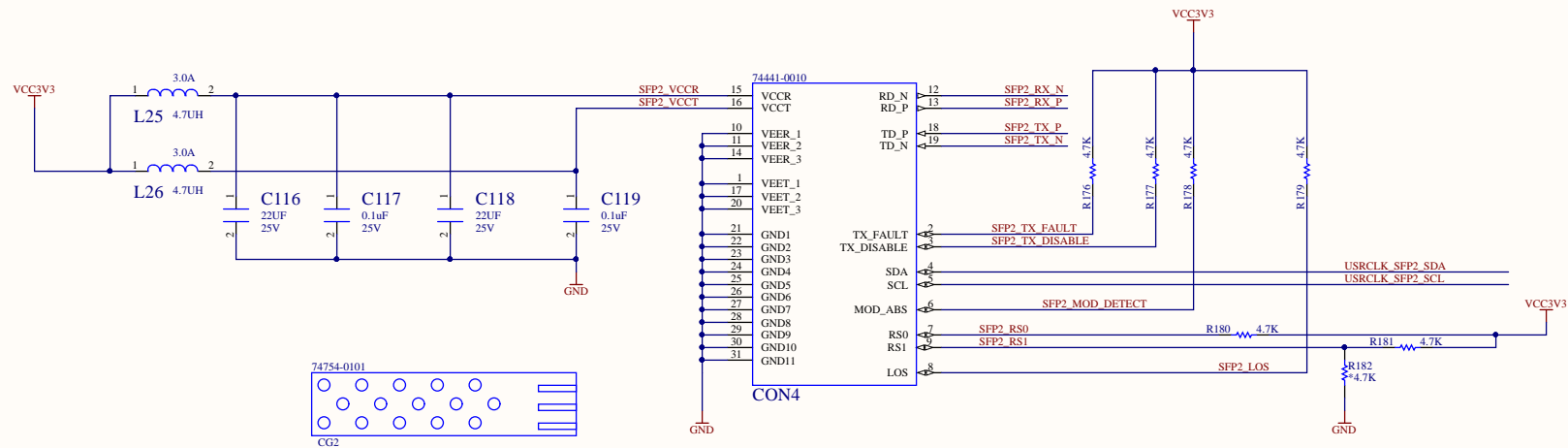
Company: FH	Title: USB_HUB	of PE7030
Date: 2019-07-20	Time: 3:46:07 PM	Engineer: WG RJ
Revision: V3	Sheet: 21	of 42
		Size: B+



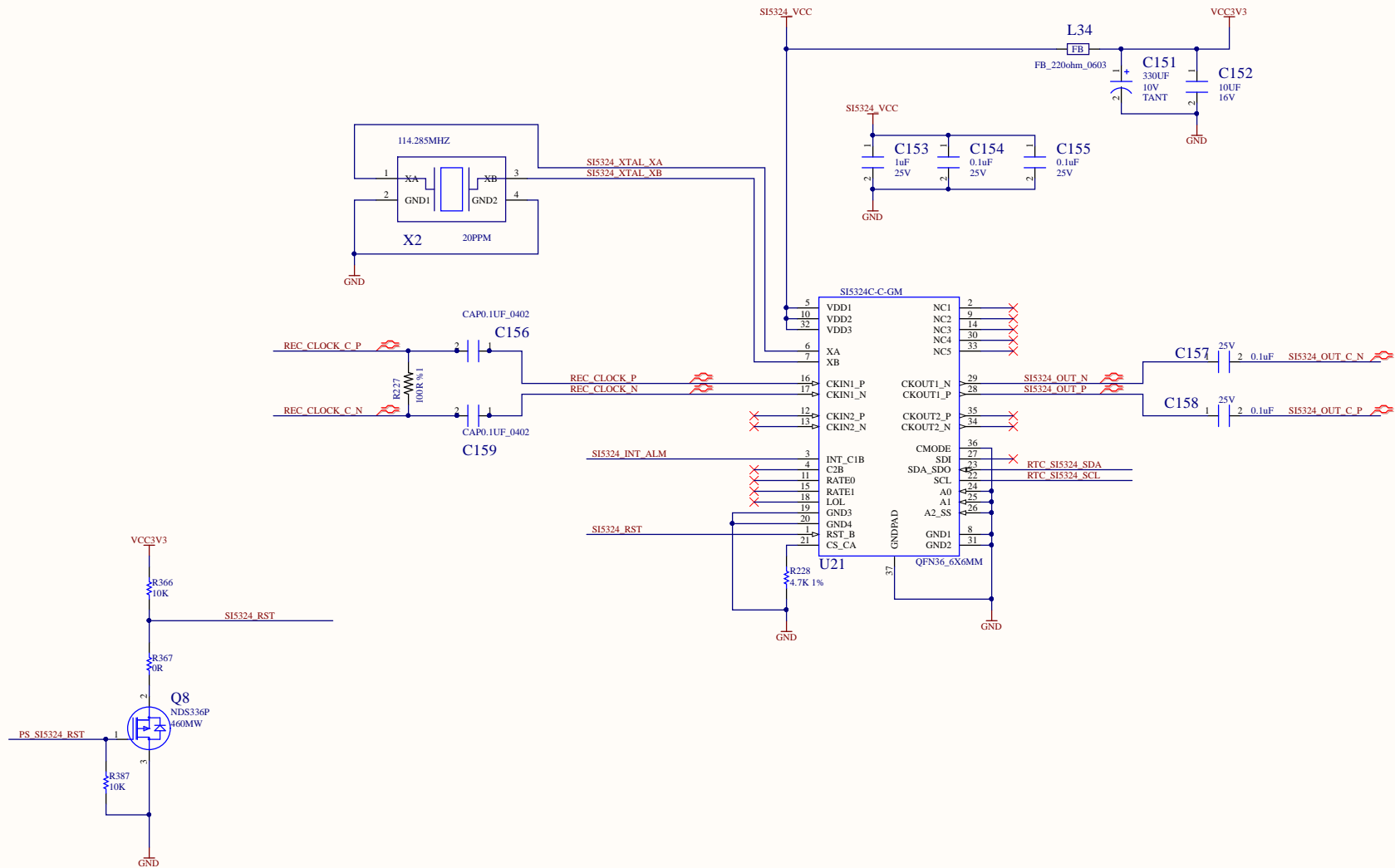
Company: FII	Title: Oscillator	of PE7030
Date: 2019-07-20	Time: 3:46:07 PM	Engineer: WG RJ
Revision: V3	Sheet: 22	of 42
		Size: B+



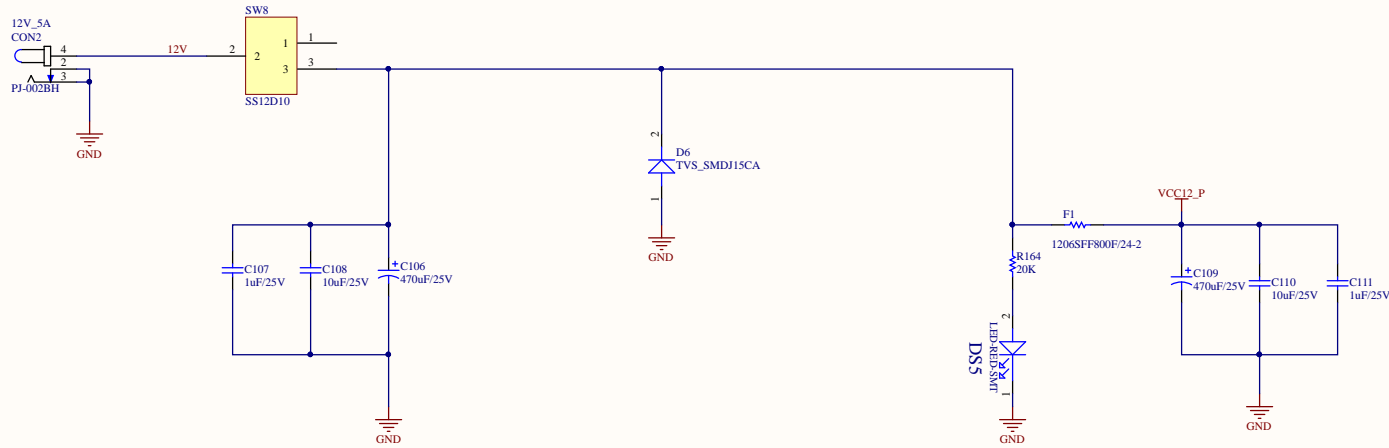




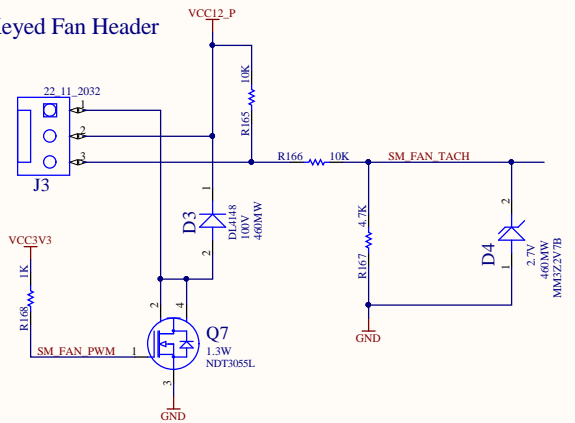
Company: FII	Title: Optical_transceiver2	of	PE7030
Date: 2019-07-20	Time: 3:46:07 PM	Engineer: WG RJ	Size: B+
Revision: V3	Sheet: 25	of	42

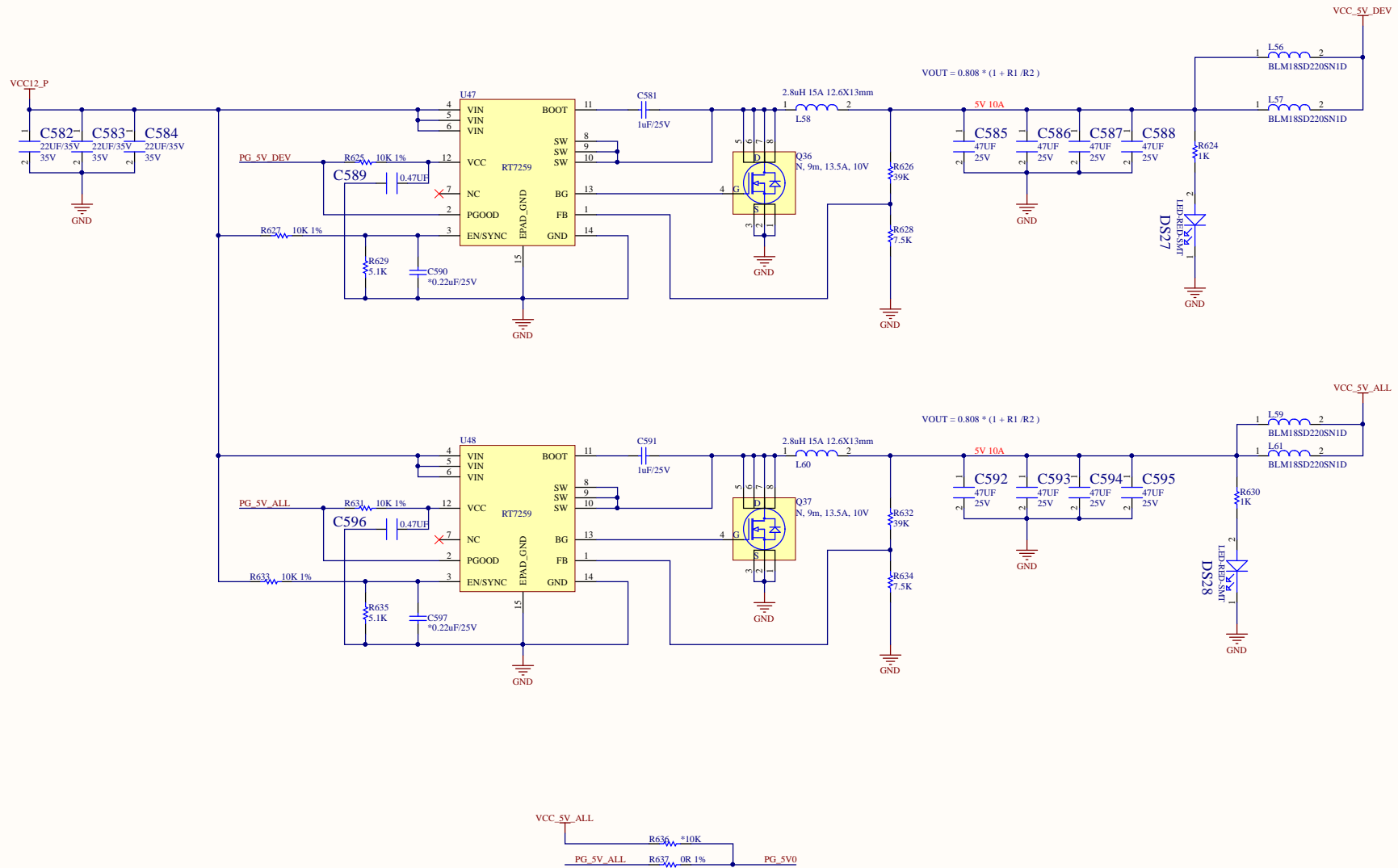


Company: FII	Title: Recovery_CLK	of PE7030
Date: 2019-07-20	Time 3:46:07 PM	Engineer: WG RJ
Revision: V3	Sheet 26	of 42
		Size: B+

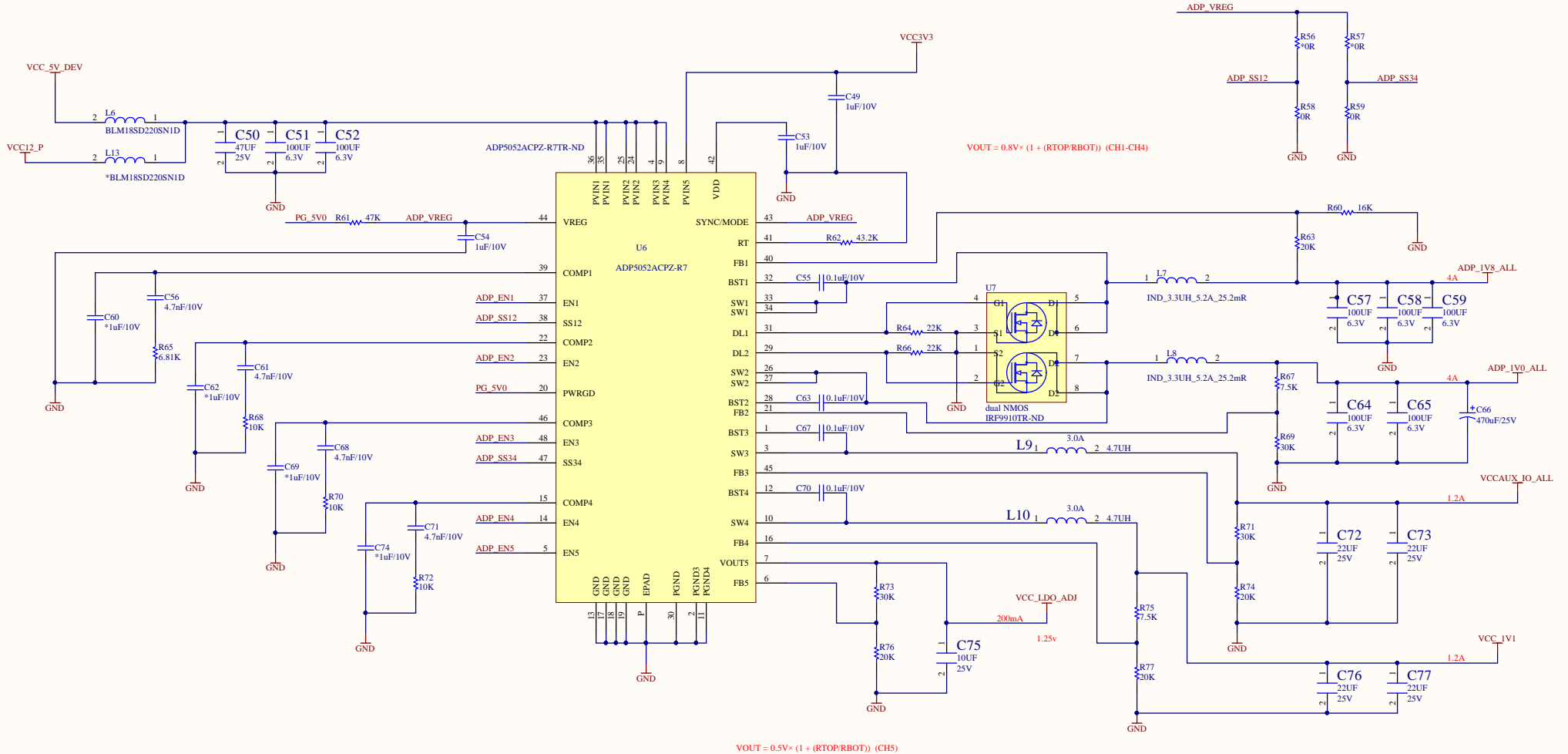


Keyed Fan Header

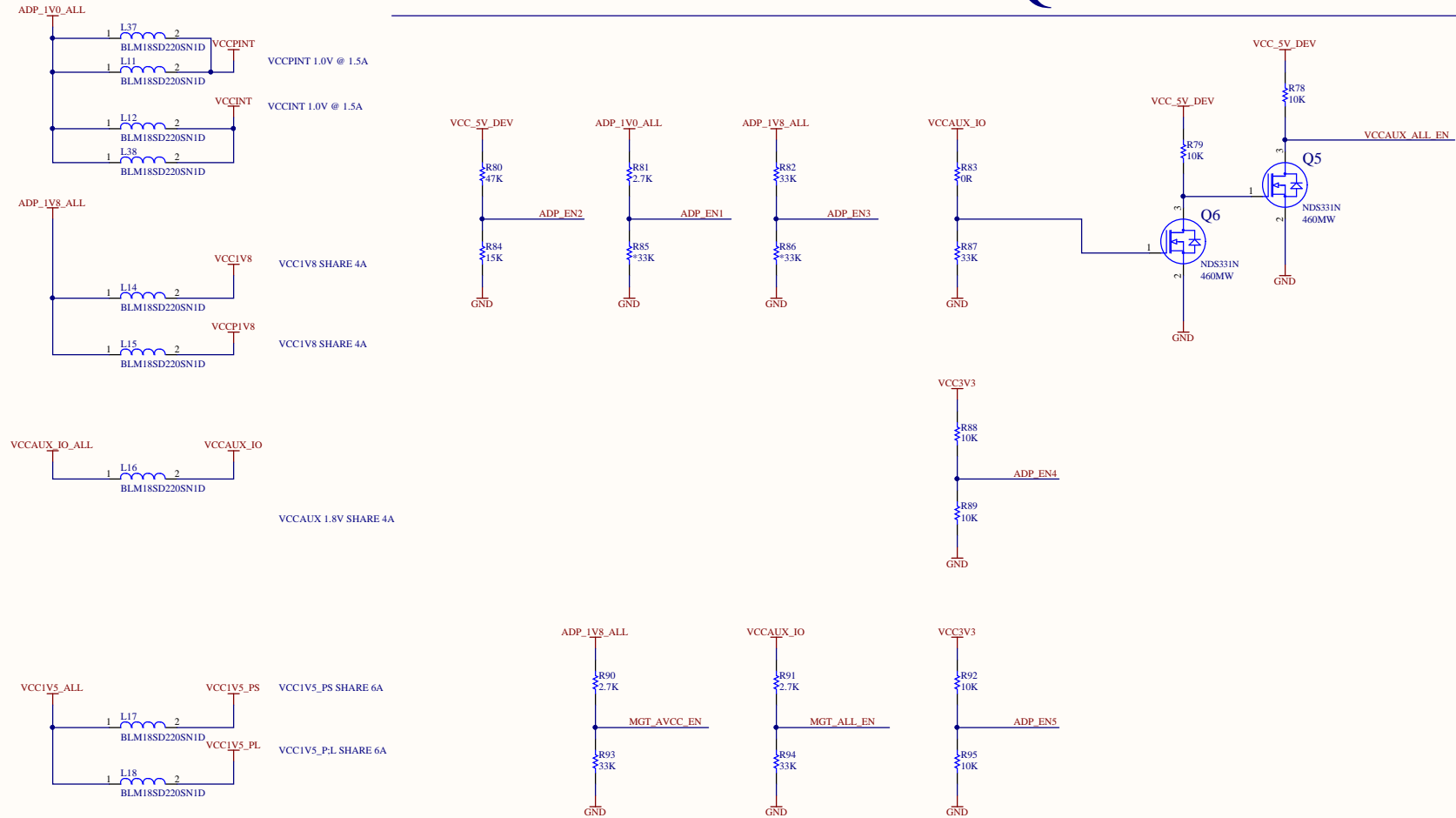


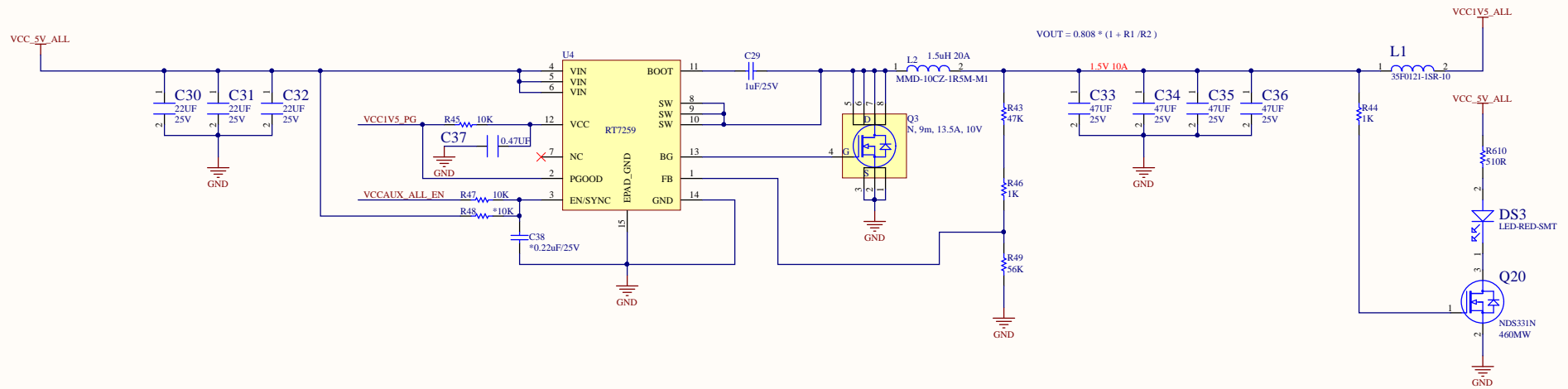


Company: FII	Title: POWER_5V	of PE7030
Date: 2019-07-20	Time: 3:46:07 PM	Engineer: WG RJ
Revision: V3	Sheet: 28	of 42
		Size: B+

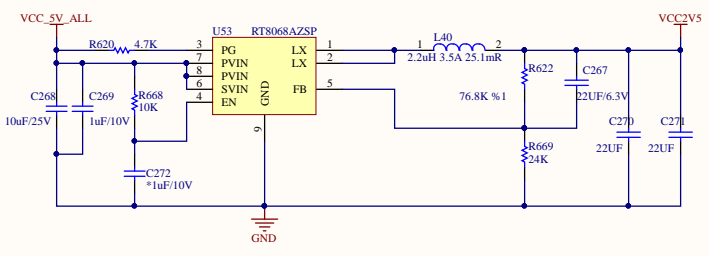
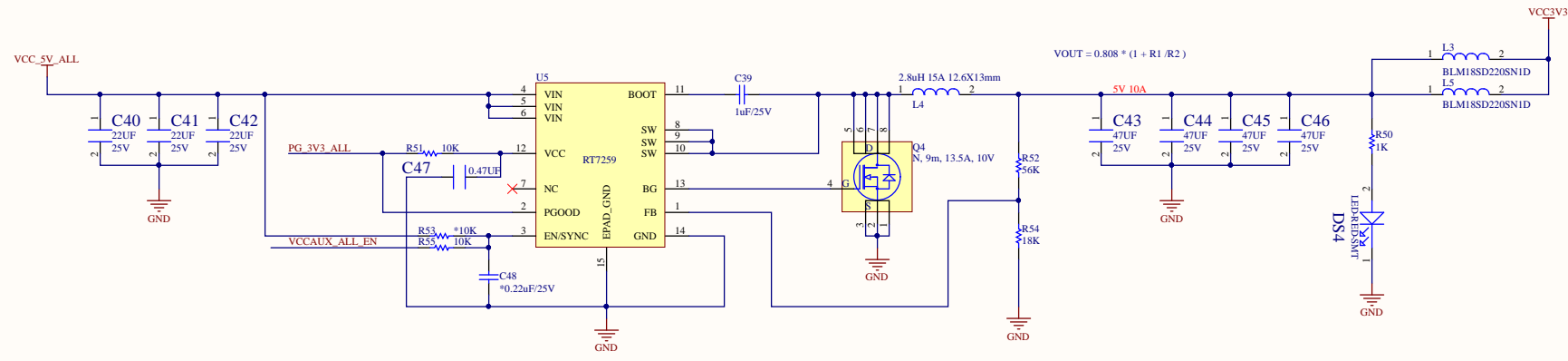


POWER SUPPLY SEQUENCE

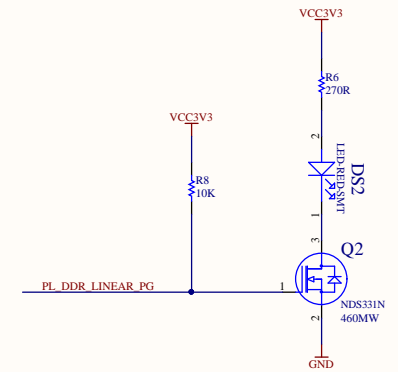
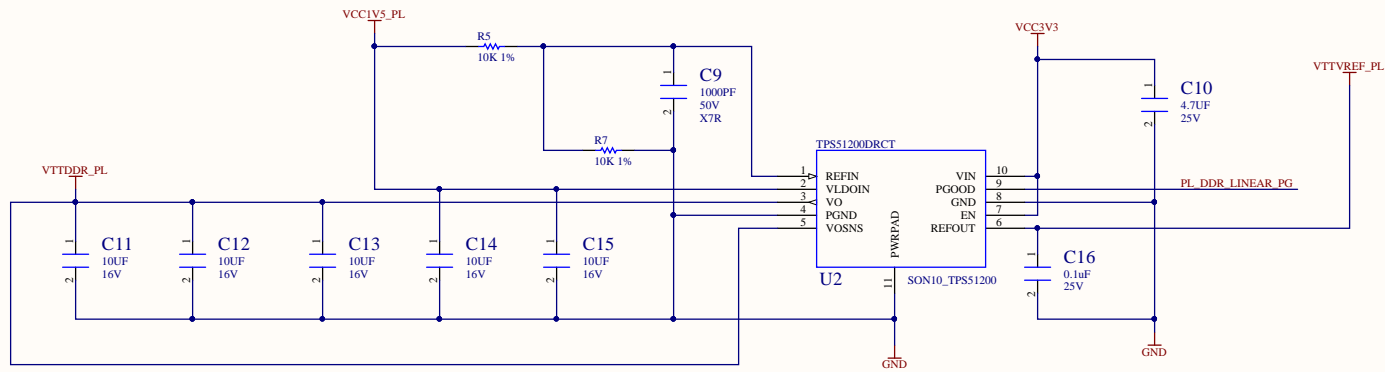
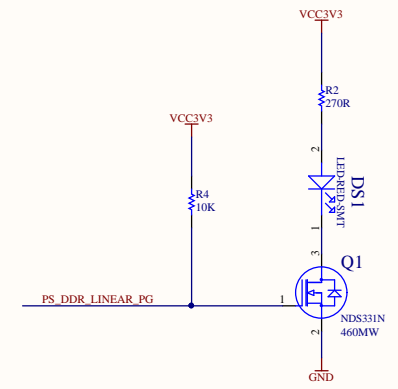
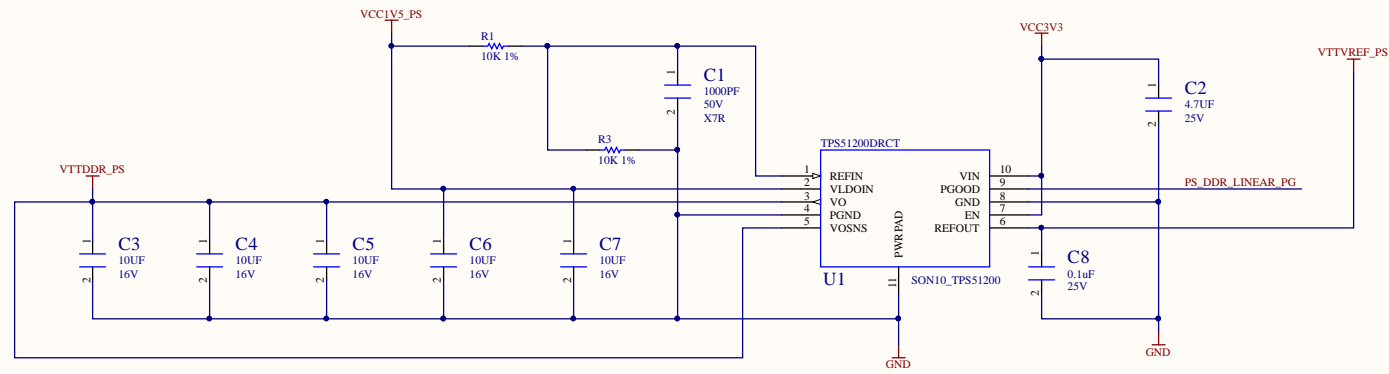


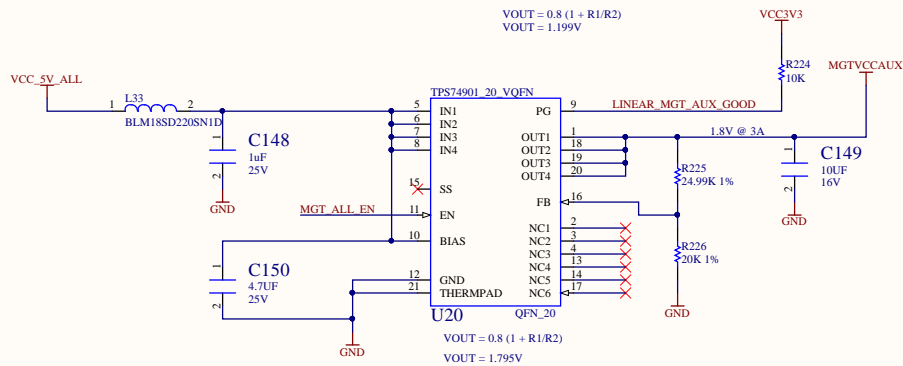
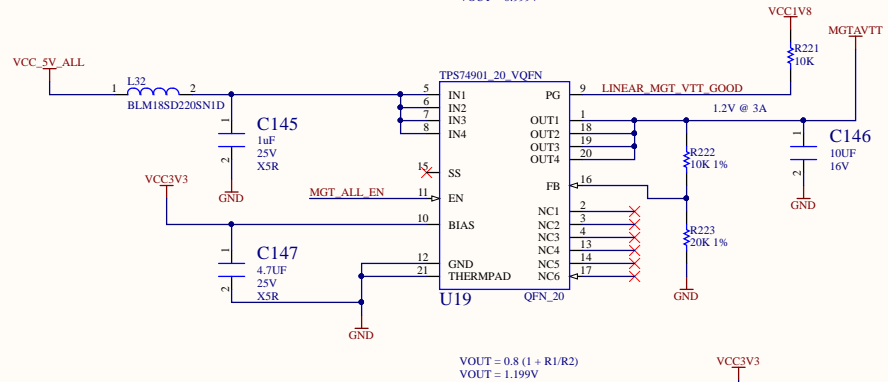
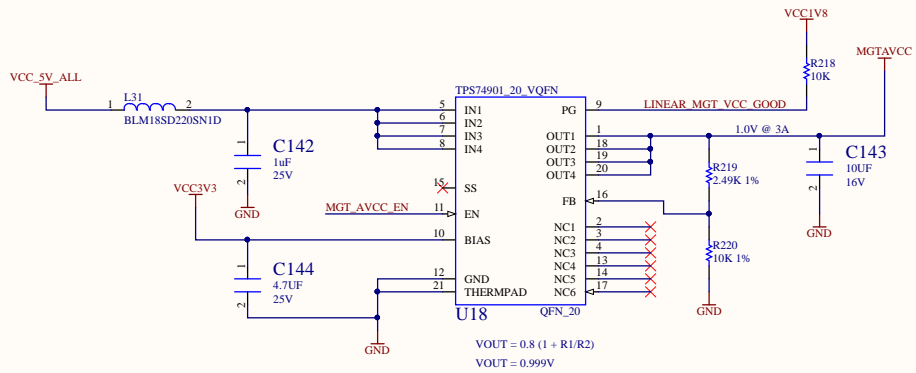


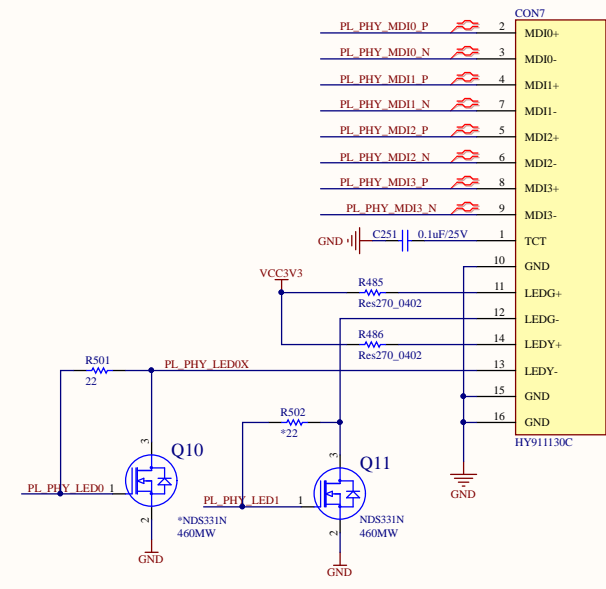
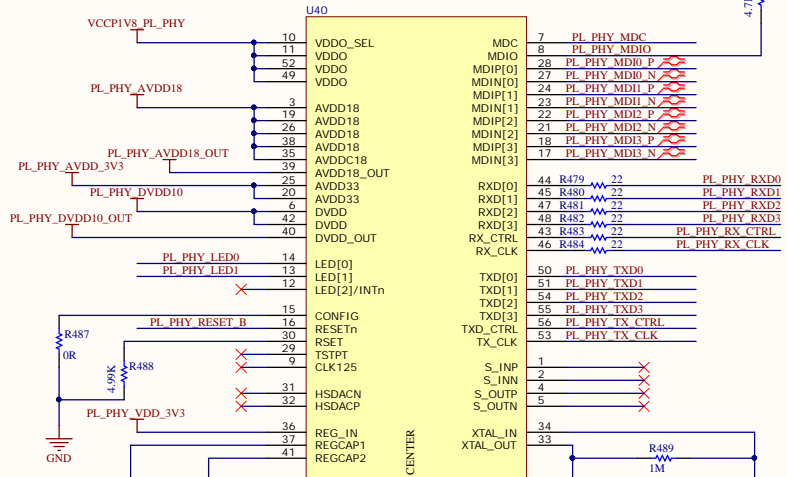
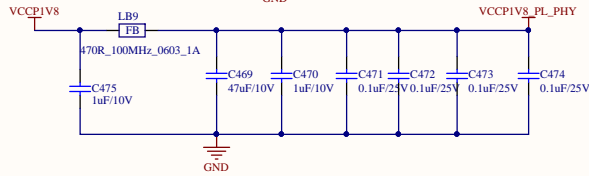
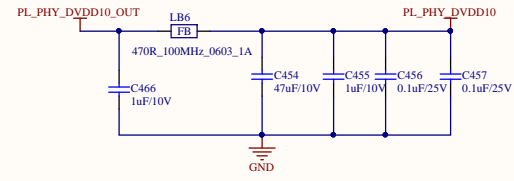
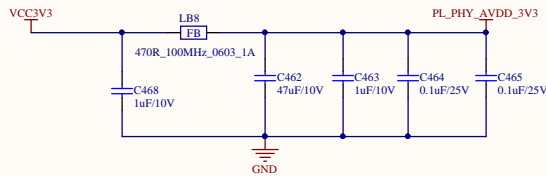
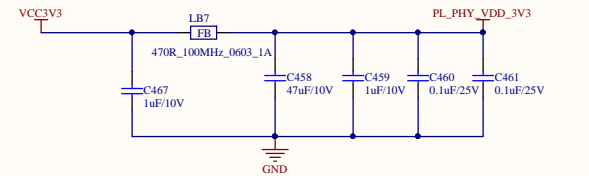
Company: FH	Title: FPGA_VCC1V5_6A	of PE7030
Date: 2019-07-20	Time 3:46:08 PM	Engineer: WG RJ
Revision: V3	Sheet 31	of 42
		Size: B+



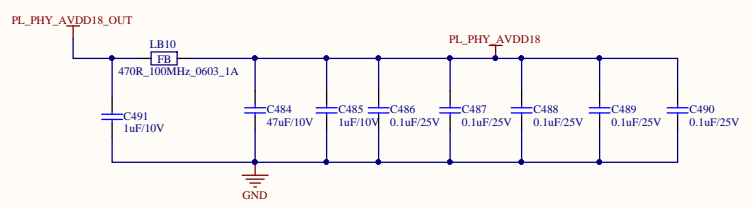
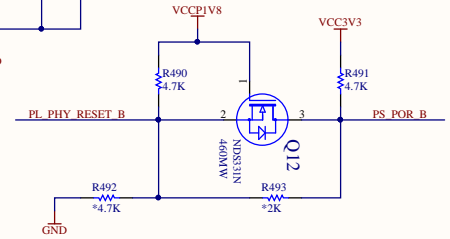
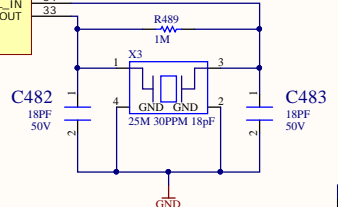
Company: FII	Title: FPGA_VCC_3V3	of	PE7030
Date: 2019-07-20	Time: 3:46:08 PM	Engineer: WG RJ	Size: B+
Revision: V3	Sheet: 32	of	42

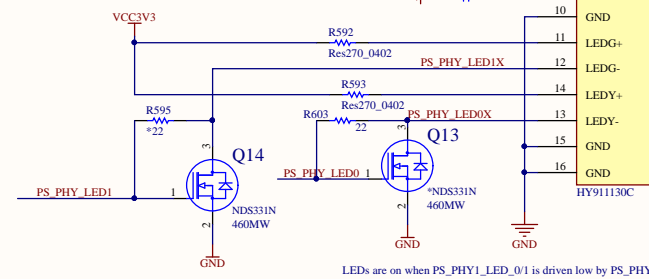
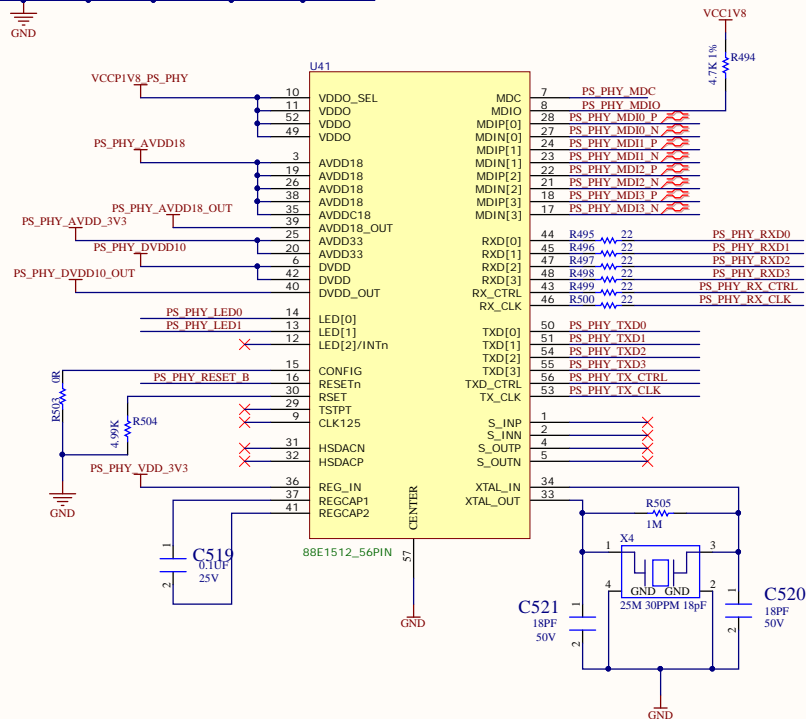
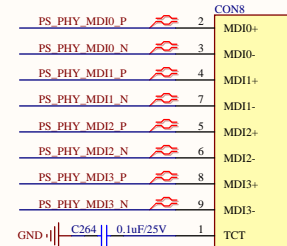
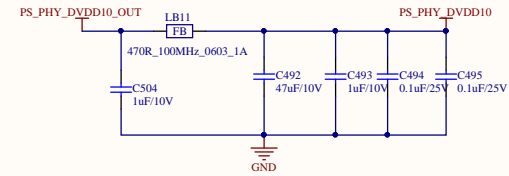
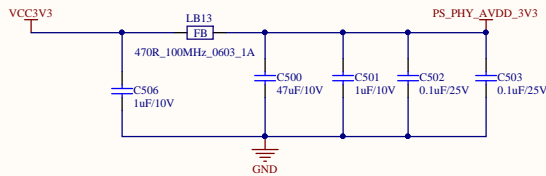
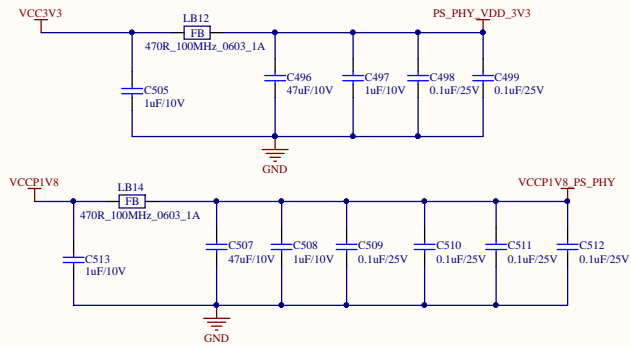




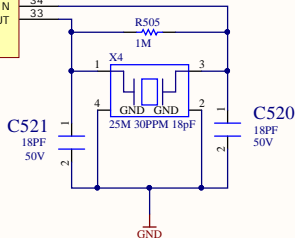
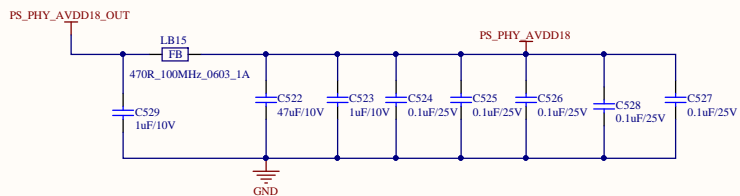


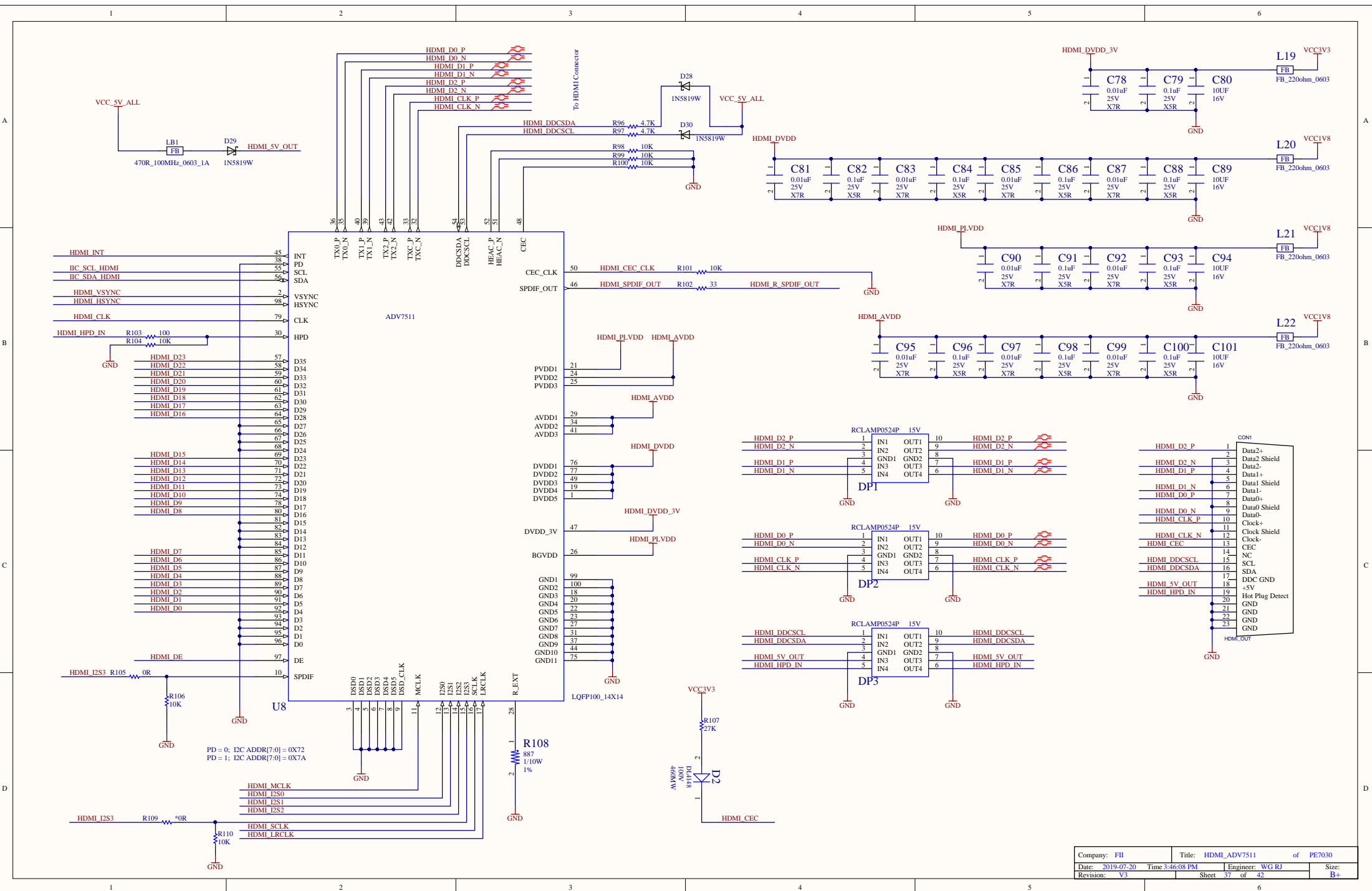
LEDs are on when PL_PHY1_LED_0/1 is driven low by PL_PHY

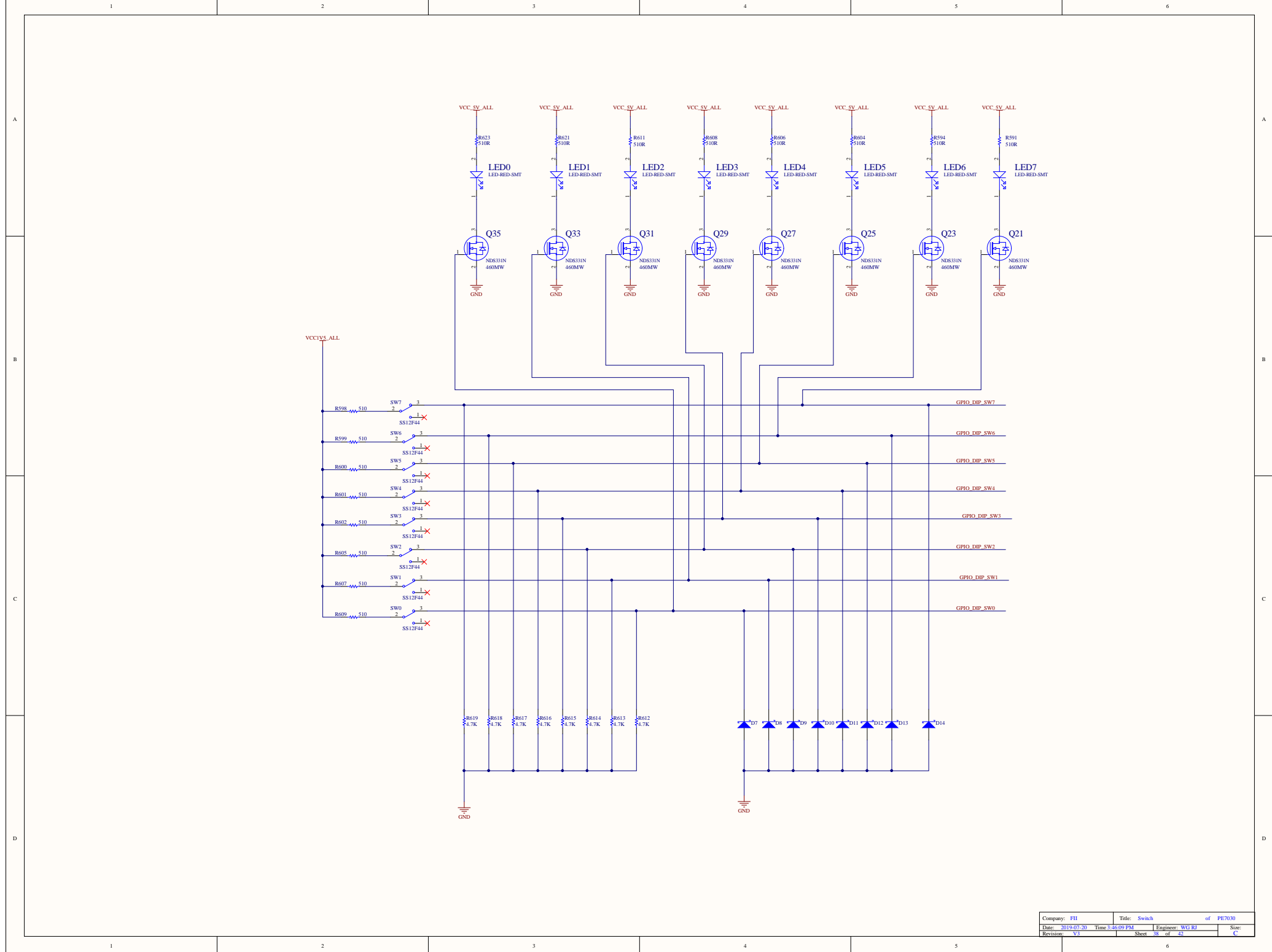


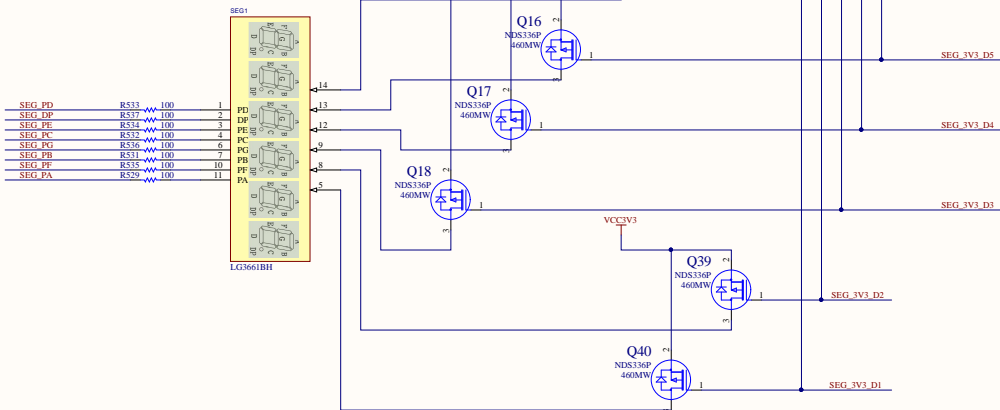
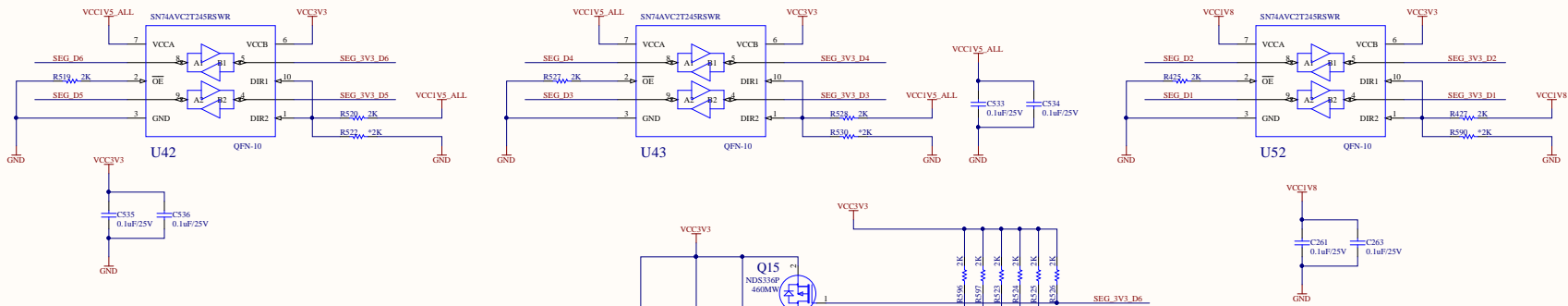
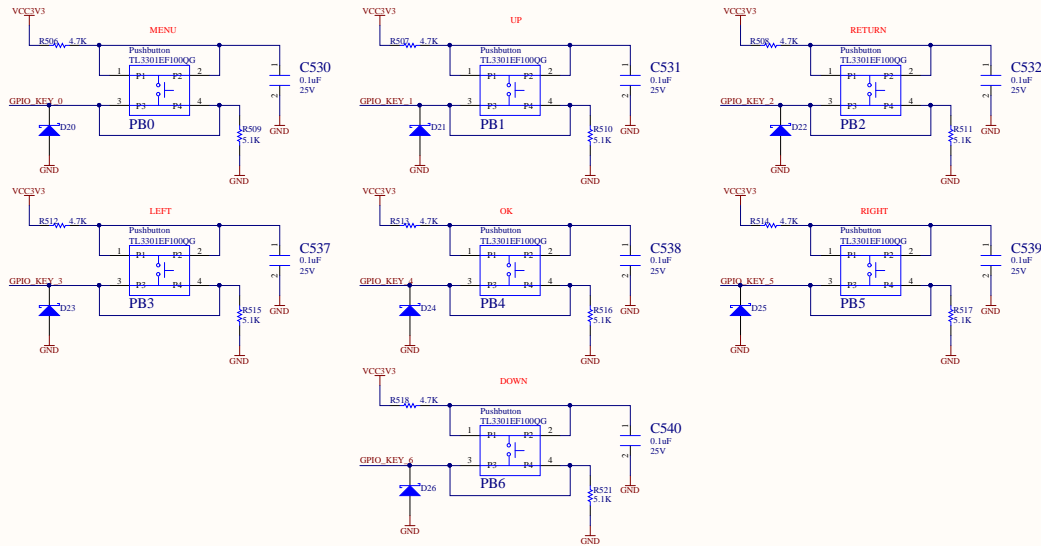


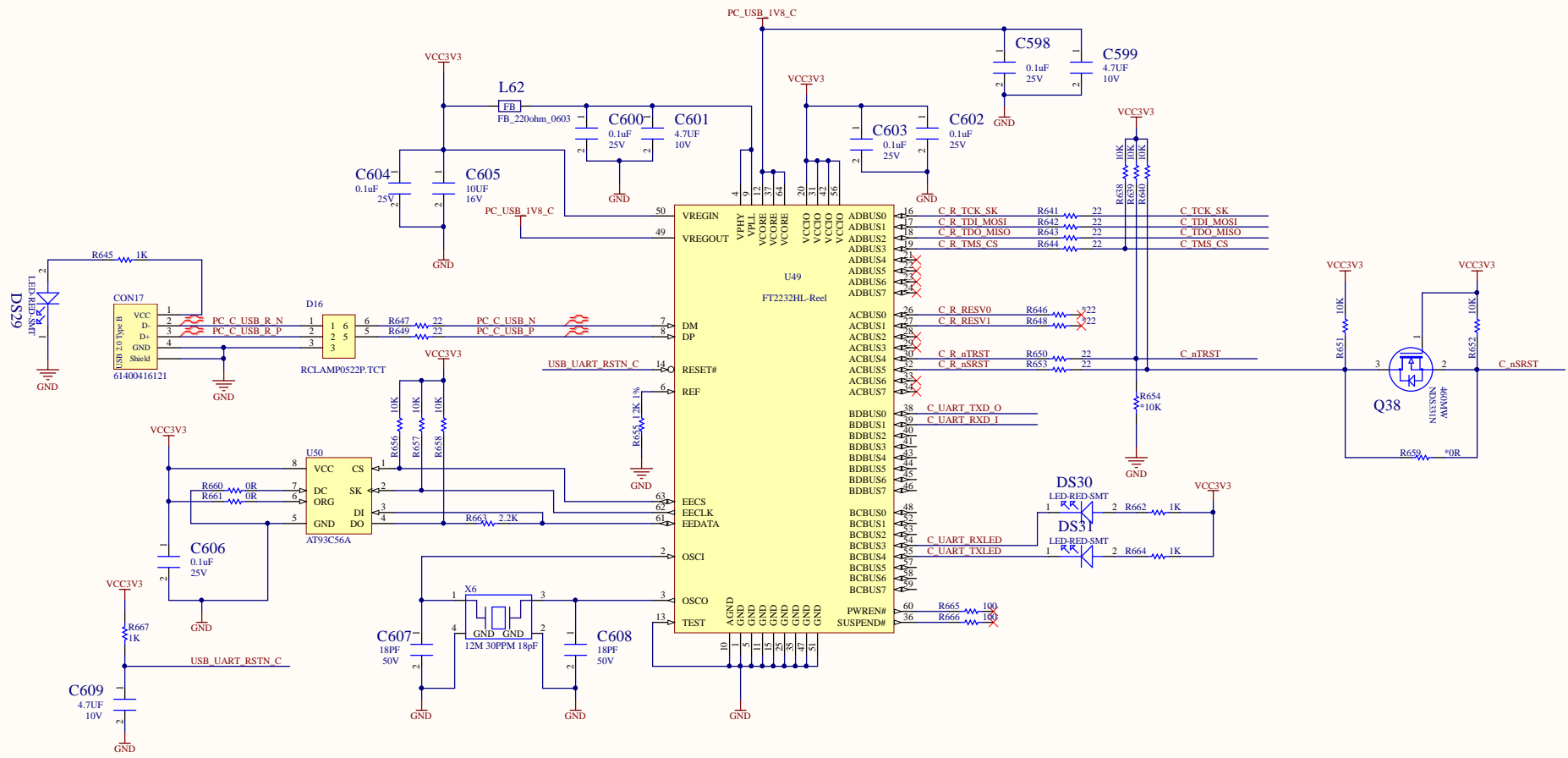
LEDs are on when PS_PHY1_LED_0/1 is driven low by PS_PHY

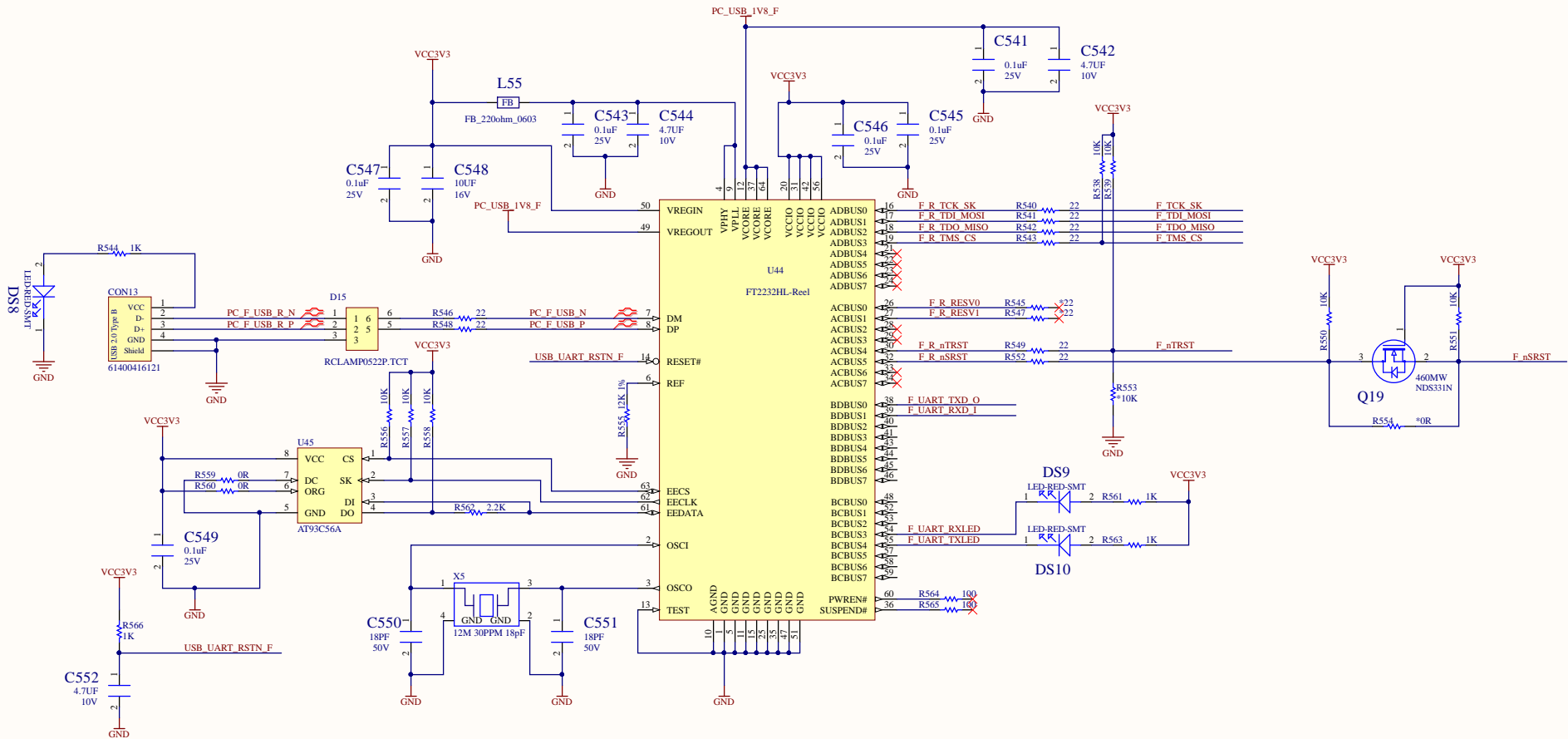








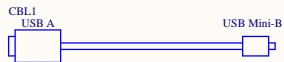




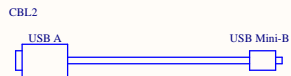
Company: FII	Title: usb_2_uart	of PE7030
Date: 2019-07-20	Time 3:46:09 PM	Engineer: WG RJ
Revision: V3	Sheet 41	of 42
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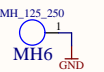
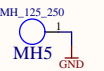
- 1) Modify USB_RESET_B_AND from mio 7 -> mio 0
- 2) Moidyf SI5324_RST from PL pin K6 to PS mio 7
- 3) Change usb hub oscillator from VCC_1V8 TO VCC1V8
- 4) Change SFP1_LOS, SFP1_MOD_DETECT, SFP1_TX_DISABLE from PL to PS
- 5) Change SFP2_TX_DISABLE, SFP2_LOS from PL to PS



USB Mini-B Cable
USB_MINIB_CABLE



USB Micro-B Cable
USB_MICRO_CABLE



Company: FH	Title: Mechanical	of PE7030
Date: 2019-07-20	Time 3:46:09 PM	Engineer: WG RJ
Revision: V3	Sheet 42 of 42	Size: B+