FII-PRX100 Hardware Configuration

V1.0

FRASER INNOVATION INC

Version Control

Version	Date	Description
1.0	07/11/2019	Initial Release

Copyright Notice:

Thank you for purchasing the FPGA development board. Please read the manual carefully before using the product and make sure that you know how to use the product correctly. Improper operation may damage the development board. This manual is constantly updated, and it is recommended that you download the latest version when using.

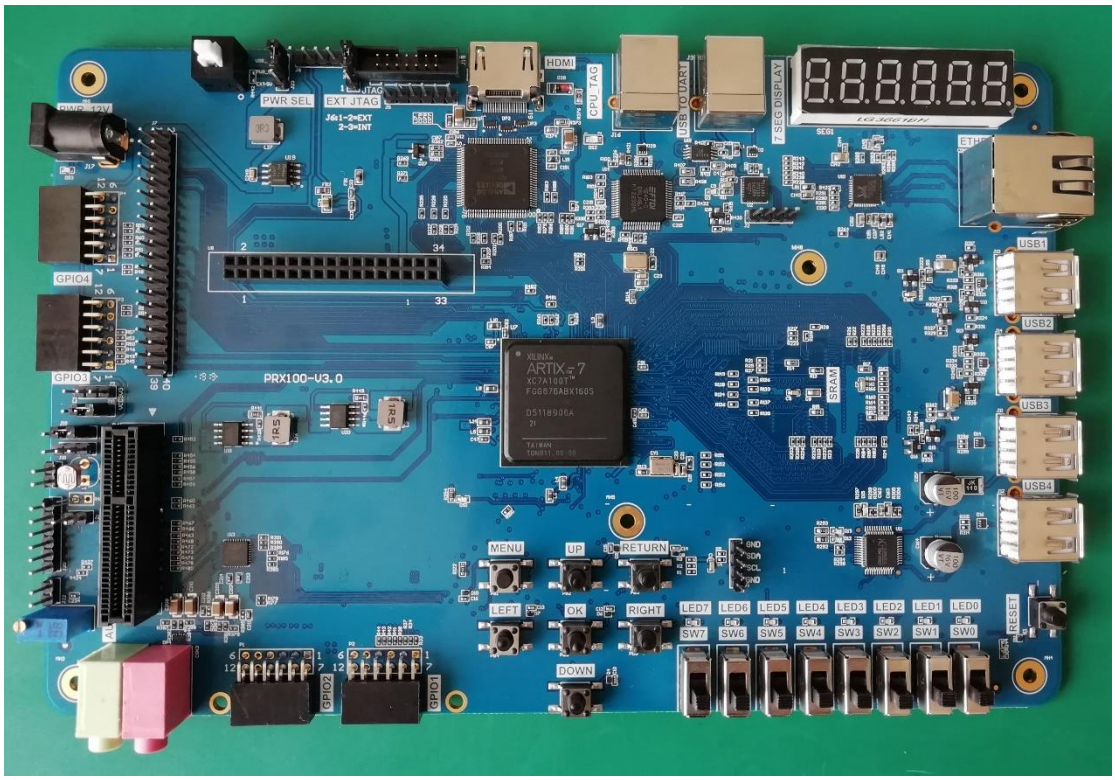
Official Shopping Website:

https://fpgamarketing.com/FPGA-JTAG-ALTERAJTAG.htm

Contents

1. Introduction 5
2. Basic Features 10
1) FPGA 10
2) Power Supply Interface 10
3) Segment Display Decoders 15
4) HDMI Interface 18
5) EEPROM AT24C02 20
6) Gigabit Ethernet Interface 21
7) Push Button 24
8) AD/DA Thermistor, Photoresistor and Potentiometer 26
9) Toggle Switch 28
10) LED 30
11) Configuration Chip FLASH 31
12) GPIO (PMOD) Expansion Interface 31
13) JTAG Interface 34
14) UART Interface 36
15) SRAM 38
16) Audio 42
17) USB Keyboard and Mouse Interface 43
18) TFT LCD Interface 46
19) 40-pin Extended GPIO Interface 48
20) PCIE Interface 49
3. References 53

Fraser Innovation Inc develops FII-PRX100 based on the boards of the Xilinx ARTIX-7 series. It was initial released in 2018. This development board is resource-rich and high-speed, making it an ideal platform for learning and engineering research. This development board has been spent a lot on system design, PCB design, and function creation. It could even be said comprehensive and powerful.



PRX100 Development Board Full View

1. Introduction

FII-PRX100 uses Xilinx's ARTIX-7 series chip, model XC7A100T-2FGG676I, which is currently Xilinx's latest generation FPGA device.

The Artix-7 is one of the Xilinx 28nn FPGA families. It features a small form factor package that reduces the power consumption of the Artix-7 family by half compared to the Spartan-6 family.

PRX100 system block diagram:

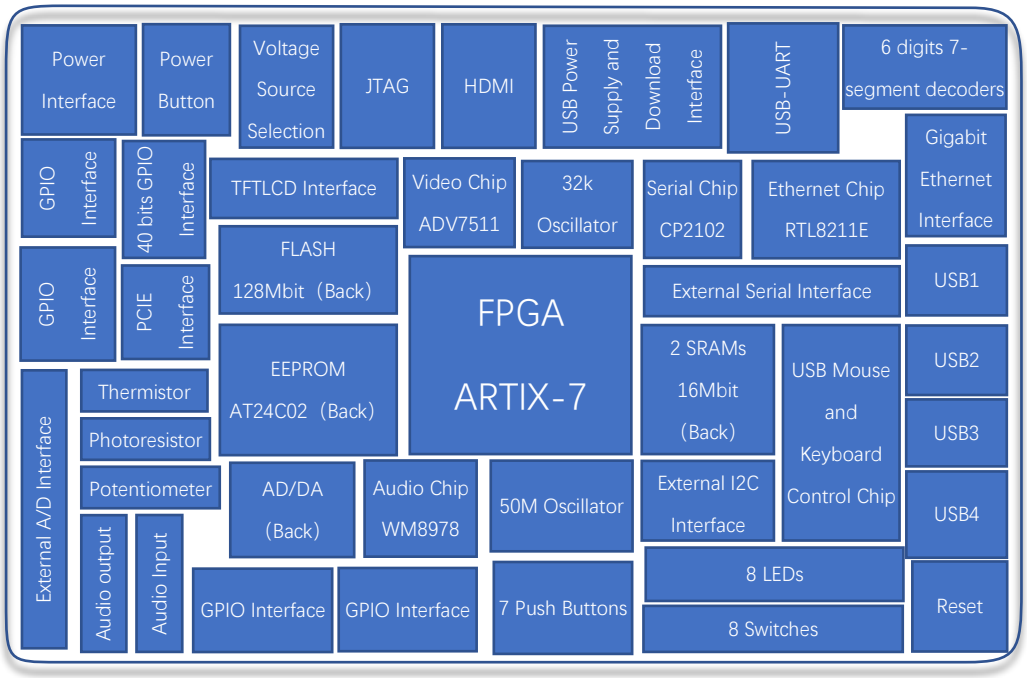


Figure 1 PRX100 System Block Diagram

Hardware resources:

- It can be powered by external 12V DC source or by "USB Power Supply and Download Interface". The latter also provides program download functionality. Only one wire is to complete the power supply and download functions;

- 6 digits comment anode 7-segment decoders, through dynamic scanning to achieve data display;
- 1 HDMI interface displaying color pictures or camera video;
- 1 chip I2C interface EEPROM chip, model AT24C02;
- 1 Gigabit Ethernet interface;
- 8 push buttons, 7 for programmable buttons, 1 for reset button;
- 1 photoresistor, through which it can simulate light control; 1 thermistor, which can collect temperature or analog temperature alarm function; 1 potentiometer, which can simulate voltage change;
- 1 PCF8591 AD/DA conversion chip, reserved external interface, free input and output;
- Onboard 50MHz and 32.768kHz oscillators provide stable clock signals to the development board;
- 8 switches;
- 8-bit LED light-emitting diodes;
- 1 128Mbit Flash chip;
- 4 GPIO external signal expansion interfaces, also the PMOD standard interface;
- A 40-pin GPIO expansion interface that provides a large amount of I/O for developers to use freely;

- Two JTAG interfaces, one for the FPGA download debug interface and one for the RISC-V CPU JTAG debug interface. Built-in RISC-V CPU software debugger, no external RISC-V JTAG emulator required;
- 1 UART asynchronous serial interface;
- 2 SRAMs with a capacity of 16Mbit;
- a pair of audio input and output interfaces;
- 1 PCIE interface;
- 4 USB interfaces, 2 for the mouse and keyboard interface, 2 for the universal serial interface;
- 1 USB (USB-B) to UART interface for serial communication;
- 1 TFTLCD touch screen interface, which can realize the display and operation of the touch screen;

Note: Before using development board, you need to check the following

1) Power supply jumper J23. If you are using an external power supply interface, use a jumper cap to connect the two jumpers "EXT_5V" and "PWR_5V". If you are using the "CPU_TAG" interface to supply power, please connect "USB_5V" and "PWR_5V". As shown below:

Figure 1.2 External Power Supply Interface

Figure 1.3 USB Power Supply and Download Interface

Figure 1.4 Power Selection Jumper J23

2) Part of the FPGA BANK voltage is determined by selection jumpers J9, J10. Voltage of BANK34 and BANK35 in evelopment board, in order to adapt to a variety of external signals, is adjustable power supply, specifically by two common voltage options, 1.8V and 3.3V. Before the development board works, please make sure that the jumpers of J9 and J10 are connected. By default, you will be connected to 3.3V. As shown below:

Figure 1.5 BANK Voltage Selection

3) The program download selection is jumper J6. The development board has two kinds of program download methods, one is to use the external downloader to connect to the JTAG interface to download; the other is to use the provided USB cable to connect to the "CPU_TAG" interface to download. J6 decides which way to use it. J6 1-2 connection is downloaded using the JTAG interface, and connection 2-3 is downloaded using the USB cable. As shown below:

Figure 1.6 Program Download Selection Jumper J6

2. Basic Features

The schematics quoted in this article are intended to highlight the key points, and the circuits that are not related to the theme (such as protection circuits or filter circuits) will be eliminated. Please pay attention to that. For the source material, please refer to the attached schematic.

1) FPGA

As mentioned above, this development board FPGA model is XC7A100T-2FGG676I, which is the latest generation of high-performance FPGA of Xilinx.

Figure 2.1 FPGA Physical Picture

Resource	Device
	XC7A100T-2FGG676I
Logic Cells	101,440
Logic Units	63,400
Maximum Number of User I/Os	300
Maximum Operating Supply Voltage	1.05V
Minimum Operating Supply Voltage	0.95V
Number of Registers	126,800
Operating Temperature	-40 to 100 °C
Pin Count	676
RAM Bits	4,976,640 Bit
Supplier Package	FCBGA

Figure 2.2 Chip Resources

2) Power Supply Interface

The development board has two power supply modes, one is for external 12V DC power supply. (please use the power supply that comes with the development board, do not use other specifications of the power supply to avoid damage to the development board) Its power supply interface is as follows:

Figure 2.3 External Power Supply Interface

The second way is to use the USB cable to connect the "CPU_TAG" interface. See Figure 2.4.

Figure 2.4 Internal Power Supply Interface

It should be noted that regardless of the power supply method, the power selection jumper needs to be connected to the correct position. As shown below:

Figure 2.5 Power Supply Selection Jumpers

By the way to mention the power supply circuit of the development board and the power supply of the FPGA. The external 12V power supply is converted to a 5V power supply through the U19 power supply chip and connected to the pin 1

of J23. The "PC_USB5V" power supply from the USB port is connected to the pin 3 of J23. With which of the two is connected to the 2nd pin, it powers the development board. There is no problem when the two power supplies are connected at the same time.

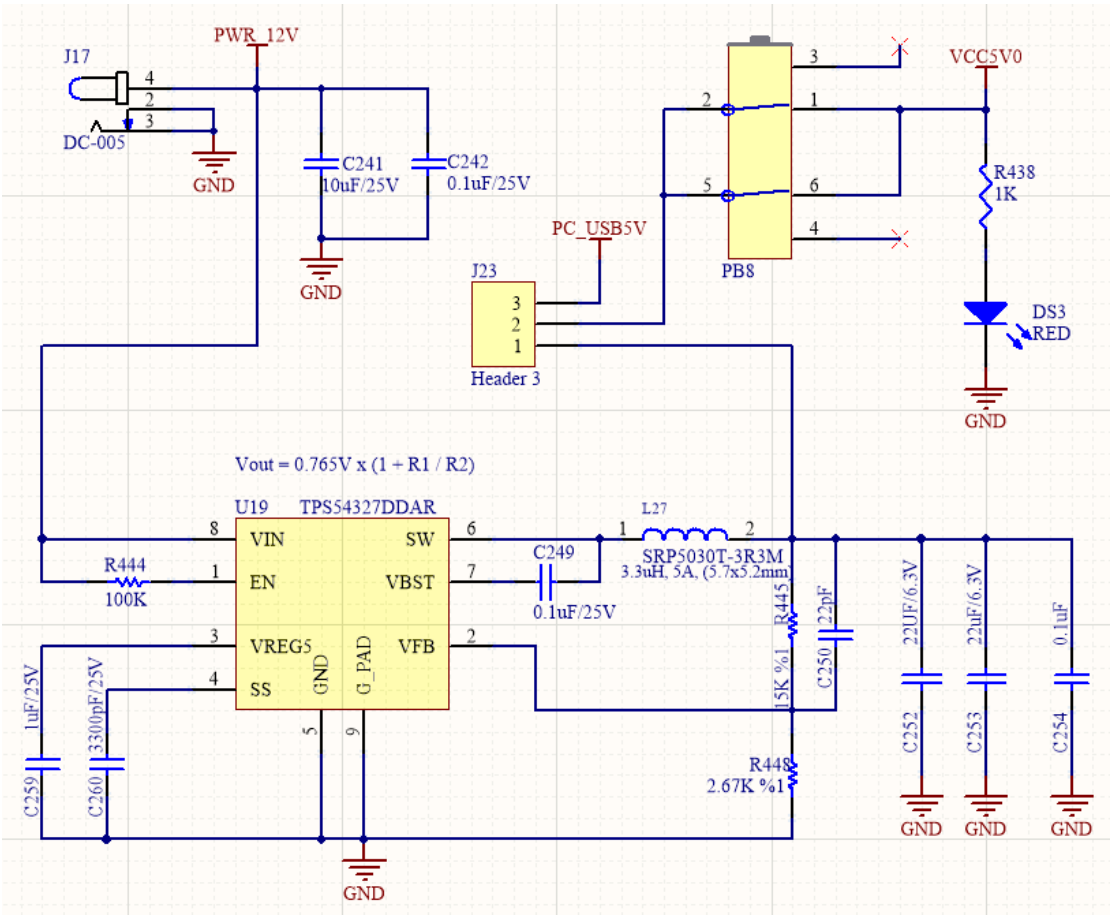


Figure 2.6 External Power Supply Schematics

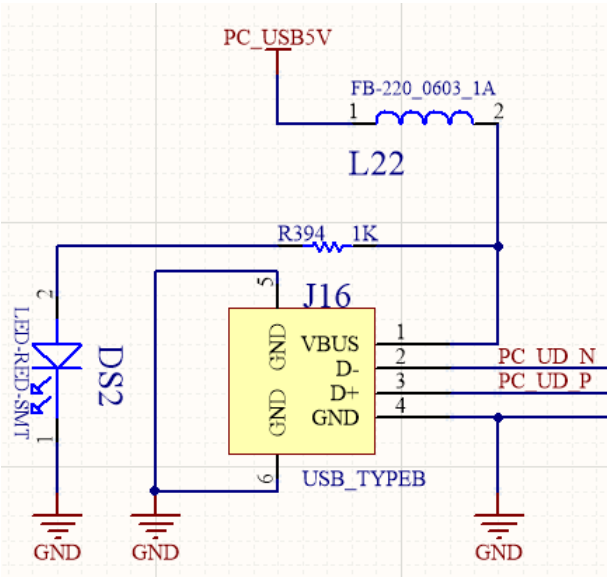


Figure 2.7 USB Power Supply Interface Schematics

We can see that after the PB8 is turned on, the power supply is connected to the VCC5V0 level network of the development board, and then converted to the 1.0V (FPGA core voltage), 1.8V or 3.3V. Among them, 1.8V and 3.3V are the BANK voltage of the FPGA. The two voltages are provided to meet the level standards of various external signals. The conversion circuit is shown below.

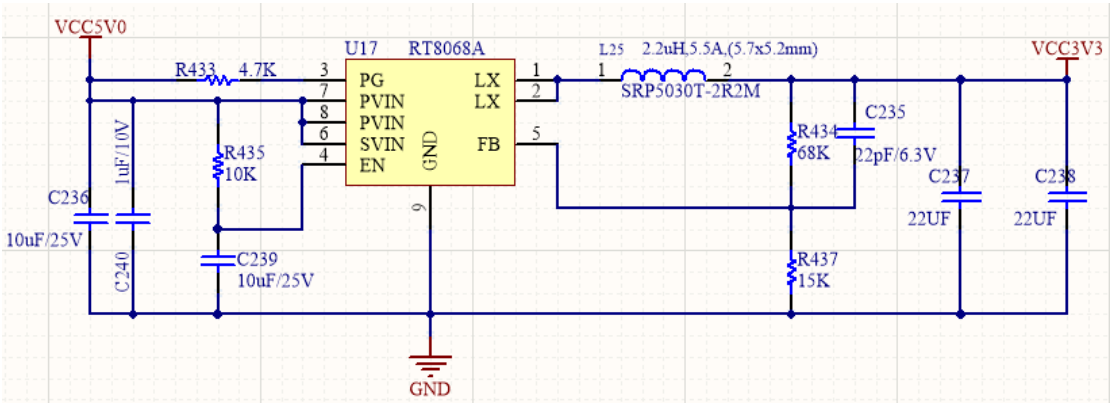


Figure 2.8 Schematics of the 3.3V Power Supply

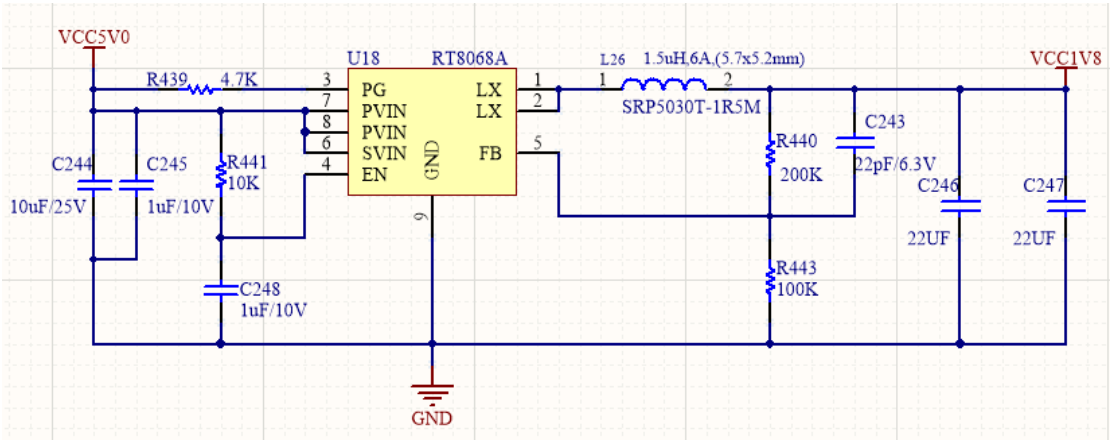


Figure 2.9 Schematics of the 1.8V Power Supply

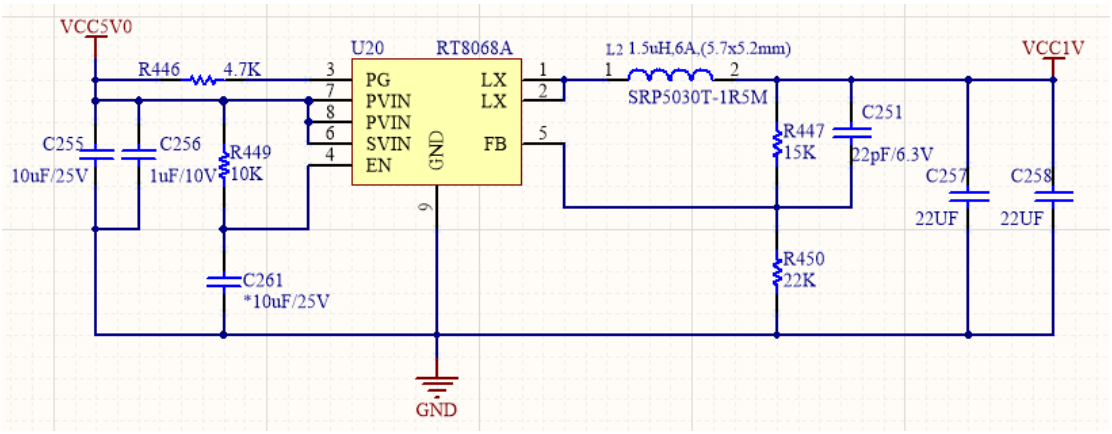


Figure 2.10 Schematics 1.0V Power Supply

If we look at the power supply of the FPGA, we can see these kinds of voltages (to highlight the topic, the screenshot skips the irrelevant circuit):

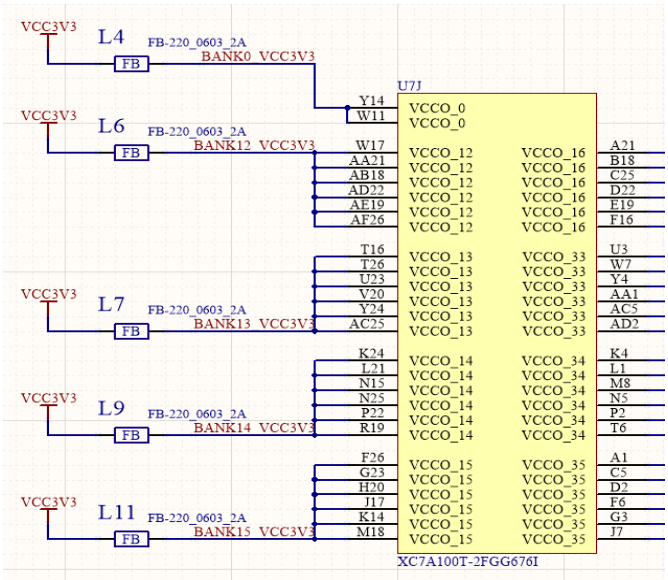


Figure 2.11 Schematics of the FPGA Power Supply 1

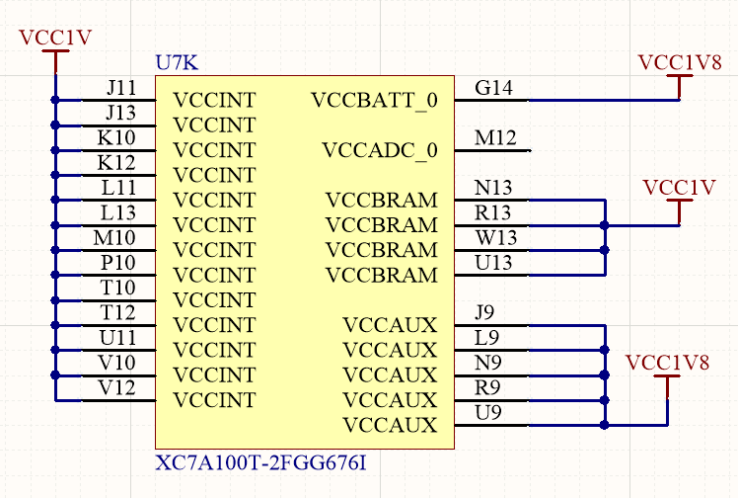


Figure 2.12 Schematics of the FPGA Power Supply 2

In Figure 2.11, 2.12, VCCO_0, VCCO_12, VCCO_13 and other pins are the BANK power pins of the FPGA. VCCINT is the core power pin of the FPGA (the other power supply parts of the FPGA are not listed. For more details, please refer to the full version schematics).

3) Segment Display Decoders

Figure 3.1 Segment Decoders

One type of digital tube is a semiconductor light-emitting device. The segment decoder can be divided into a seven-segment decoder and an eight-segment decoder. The difference is that the eight-segment decoder has one more unit for displaying the decimal point, the basic unit is a light-emitting diode. The segment structure of the decoder is shown below:

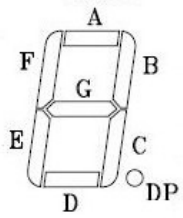


Figure 3.2 Segment Decoder Structure

We use common anode decoders. That is, the anodes of the LEDs are connected.

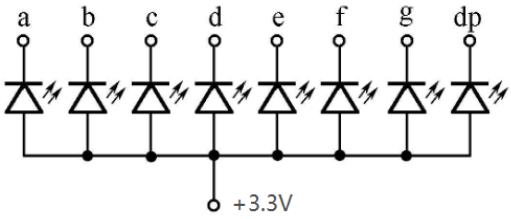


Figure 3.3 Schematics of Common Anode Decoders

To illuminate a segment of an 8-segment decoder, the level of the corresponding pin needs to be pulled low; when the pin is set high, the corresponding field will not light. This development board uses a 6-in-one eight-segment decoder. The schematics is shown below:

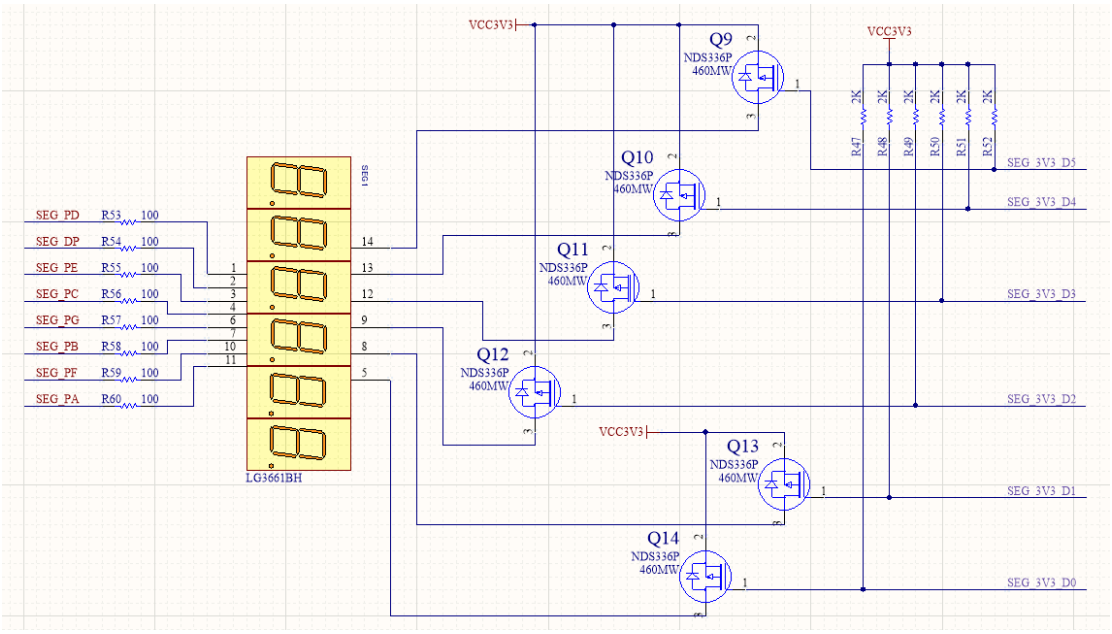


Figure 3.4 Schematic of Decoders

The six-in-one decoder is a dynamic display. Due to the persistence of human vision and the afterglow effect of the LED, although the decoders are not lit at the same time, if the scanning speed is fast enough, the impression of human eyes is a group of stable display data, no flickering can be noticed. The same segments of the six-in-one decoders are connected, a total of eight pins, and with six control signal pins, a total of 14 pins, as shown in Figure 3.4. Among them SEG_PA, SEG_PB, SEG_PC, SEG_PD, SEG_PE, SEG_PF, SEG_PG, SEG_DP correspond to the A, B, C, D, E, F, G, DP of decoder; SEG_3V3_D [0..5] are six control pins of the decoders, which are also active low. When the control pin is low, the corresponding decoder is powered, so that the LED can be lit.

Pin assignments of display decoders

Signal Name	FPGA Pin	Description
SEG PA	K26	Segment A
SEG PB	M20	Segment B
SEG PC	L20	Segment C

SEG PD	N21	Segment D
SEG PE	N22	Segment E
SEG PF	P21	Segment F
SEG PG	P23	Segment G
SEG DP	P24	Segment DP
SEG_3V3_D0	R16	Decoder 1(from right)
SEG_3V3_D1	R17	Decoder 2(from right)
SEG_3V3_D2	N18	Decoder 3(from right)
SEG_3V3_D3	K25	Decoder 4(from right)
SEG_3V3_D4	R25	Decoder 5(from right)
SEG_3V3_D5	T24	Decoder 6(from right)

4）HDMI Interface

Image display processing has always been the focus of FPGA research. At present, the image display mode is also constantly developing. The image display interface is also gradually transitioning from the old VGA interface to the new DVI or HDMI interface. HDMI is the abbreviation of High Definition Multimedia Interface. It is a digital video/audio interface technology, which is a dedicated digital interface for image transmission. It can transmit audio and video signals at the same time. The highest data transmission speed is 48Gbps (version 2.1).

The ADV7511 is a chip that converts VGA timing to HDMI timing. For details, see the related chip manual. Among them, ADV7511_Programming_Guide and ADV7511_Hardware_Users_Guide are the most important. You can configure the registers of ADV7511 by viewing this document.

Figure 4.1 HDMI Interface and ADV7511 Chip

HDMI pin assignment

Signal Name	FPGA Pin
HDMI- INT	E18
HDMI- SCL	R20
HDMI-SDA	R21
HDMI-VSYNC	A25
HDMI-HSYNC	C24
HDMI-CLK	B19
HDMI-HPD	H16
HDMI-D35	F15
HDMI-D34	E16
HDMI-D33	D16
HDMI-D32	G17
HDMI-D31	E17
HDMI-D30	F17
HDMI-D29	C17
HDMI-D28	A17
HDMI-D23	B17
HDMI-D22	C18
HDMI-D21	A18
HDMI-D20	D18
HDMI-D19	D20
HDMI-D18	A19
HDMI-D17	B20
HDMI-D16	A20

HDMI-D11	B21
HDMI-D10	C21
HDMI-D9	A22
HDMI-D8	B22
HDMI-D7	C22
HDMI-D6	A23
HDMI-D5	D21
HDMI-D4	B24
HDMI-DE	A24
HDMI-SPDIF	B25
HDMI-I2S0	B26
HDMI-I2S1	D24
HDMI-I2S2	C26
HDMI-I2S3	E21
HDMI-SCLK	E22
HDMI-LRCLK	F19

5）EEPROM AT24C02

EEPROM is generally used in the instrumentation design. It is often used as a storage for some parameters. Data is not lost when power is off, and it is easy to operate. It is an ideal storage device.

The development board contains an EEPROM, model AT24C02, with a capacity of 2kbit (256*8bit), consisting of a 256-byte block that communicates over the IIC bus. The onboard EEPROM is designed to learn how the IIC bus communicates. See Figure 5.1 for the schematics.

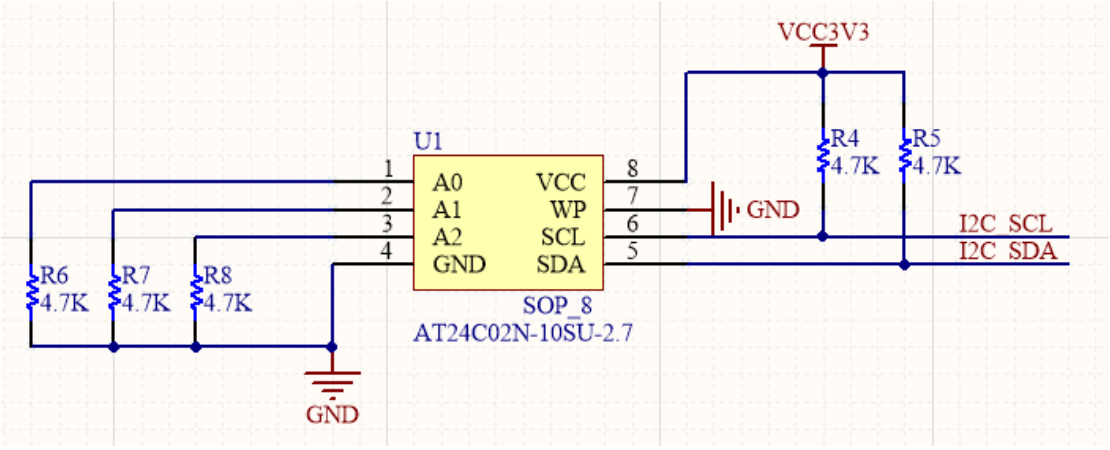


Figure 5.1 Schematics of EEPROM

This chip is located on the back of the development board, Figure 5.2 is the physical picture.

Figure 5.2 Physical Picture of EEPROM

EEPROM pin assignment

Signal Name	FPGA Pin
SDA	R21
SCL	R20

6) Gigabit Ethernet Interface

Ethernet is currently the most commonly used data communication method. Ethernet is getting faster and faster from the initial 10Mb/s to the later 100Mb/s, and to 1000Mb/s now.

The development board is equipped with an RTL8211E Gigabit Ethernet chip. The TL8211E is a highly integrated network receiving PHY chip from Realtek. It is compliant with 10Base-T, 100Base-TX and 1000Base-T IEEE802.3 standards. It can

transmit network data via CAT 5 UTP cable and CAT 3 UTP cable. It belongs to the physical layer in network communication and is used for data communication between MAC and PHY. Mainly used in network interface adapters, network hubs, gateways and some embedded devices.

The main features of the RTL8211E include:

- Meets 1000Base-T IEEE802.3ab standard
- Compliant with 100Base-TX IEEE802.3u standard
- Compliant with 10Base-T IEEE802.3 standard
- Support IEEE 802.3 RGMII interface
- Support IEEE 802.3 GMII, MII interface, only RTL8211EG support
- Support for Wake-on-LAN
- Support for interrupt function
- Support crossover detection and auto-correction
- Support half-duplex, full-duplex operation
- 1000 MHz communication CAT 5 network cable can reach 100m
- RGMII interface supports 3.3V, 2.5V, 1.8V, 1.5V signals
- LED indications for three network states are available

See below for the schematics.

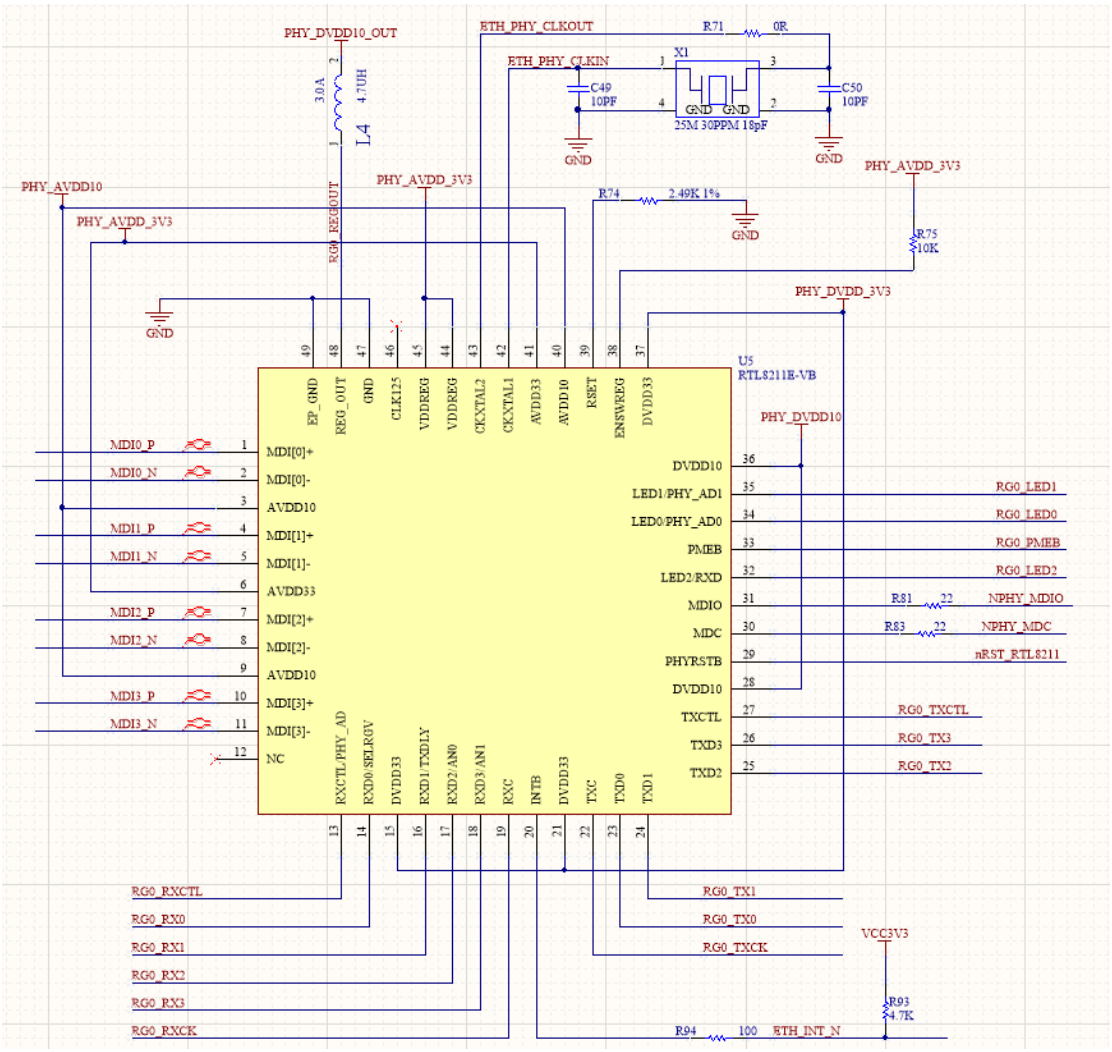


Figure 6.1 Schematics of Gigabit Ethernet Chip

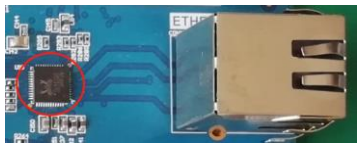


Figure 6.2 Gigabit Ethernet Physical Picture

Gigabit ethernet pin assignment

Signal Name	FPGA Pin
RG0_RXCTL	M14
RG0_RXD0	L14
RG0_RXD1	K15
RG0_RXD2	J14
RG0_RXD3	J15
RG0_RXCK	K21

RG0_TXCK	J16
RG0_TXD0	K16
RG0_TXD1	K17
RG0_TXD2	K18
RG0_TXD3	H19
RG0_TXCTL	G20
NPHY_MDC	F22
NPNY_MDIO	J20

7）Push Button

The development board has 8 push buttons, 7 of which are programmable buttons and 1 is for system reset. The default is set high and can be pressed low. Schematics is shown in Figure 7.1.

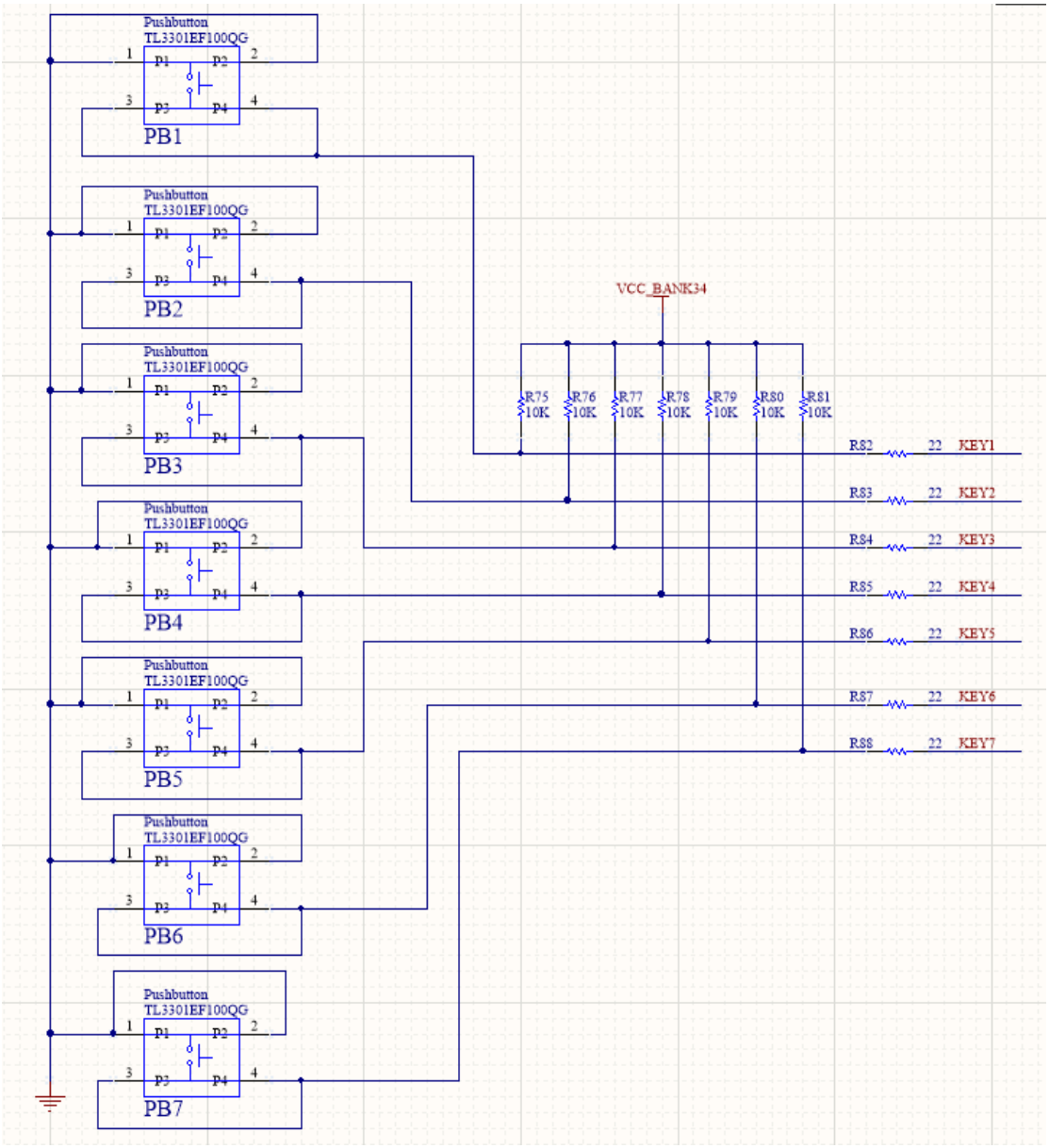


Figure 7.1 Schematics of Push Buttons

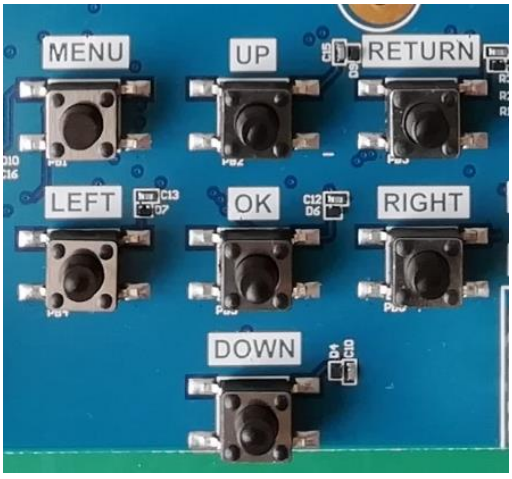


Figure 7.2 Push Button Physical Picture

Push button pin assignment

Signal Name	FPGA Pin
MENU	M4
UP	L4
RETURN	L5
LEFT	K5
OK	R1
RIGHT	P1
DOWN	R7

8）AD/DA Thermistor, Photoresistor and Potentiometer

The PCF8591 chip is a monolithically integrated, individually powered, low power consuming, 8-bit CMOS data acquisition device. It has 4 analog inputs, 1 analog output, and 1 serial I2C bus interface. The three address pins A0, A1 and A2 of PCF8591 can be used for hardware address programming (the three addresses on the development board are connected to GND, that is, the device address is 7'B1001000), allowing access on the same I2C bus. PCF8591 devices without additional hardware. The address, control, and data signals input and output on the PCF8591 device are serially transmitted over a two-wire bidirectional I2C bus. Chip features of PCF8591:

- Operating voltage range 2.5V-6V
- Low standby current
- Serial input/output via I2C bus
- I2C address selection by 3 hardware address pins

- Max sampling rate given by I2C bus speed
- 4 analog inputs configurable as single ended or differential inputs
- Auto-incremented channel selection
- Analog voltage ranges from VSS to VDD
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output

The schematics is shown in Figure 8.1 (to make the theme clearer, the figure has been modified for the design drawings):

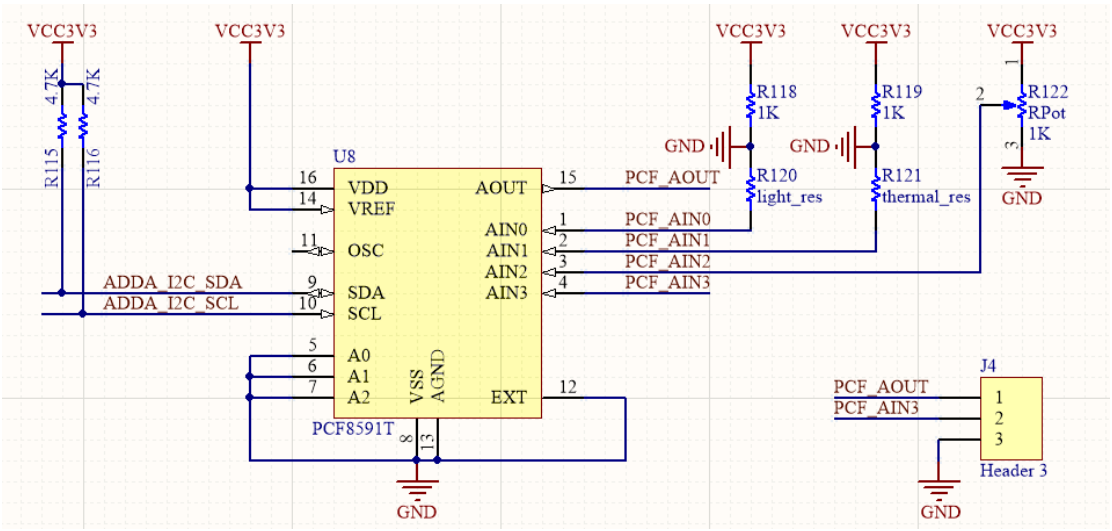


Figure 8.1 Schematics of AD/DA

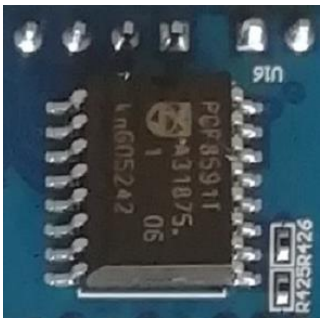


Figure 8.2 PCF8591 Physical Picture

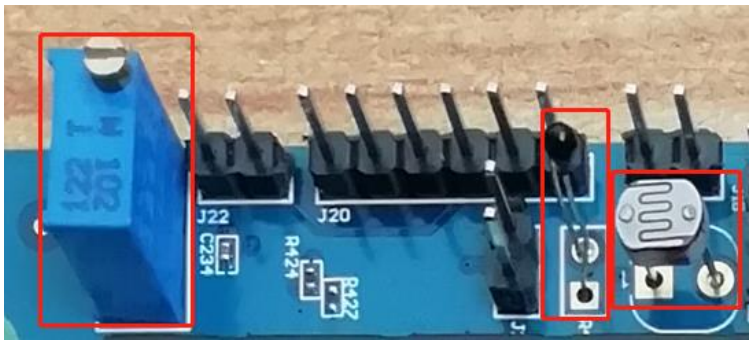


Figure 8.3 Thermistor, Photoresistor, and Potentiometer

When using a potentiometer, connect J22 with a jumper cap. When using the thermistor, connect J24. When using a photoresistor, connect J21.

PCF8591 pin assignment

Signal Name	FPGA Pin
ADDA_I2C_SAD	C19
ADDA_I2C_SCL	E20

9）Toggle Switch

The 8-bit toggle switch is onboard, and the FPGA pin gets high when the toggle switch is turned on. The schematics is shown as follows:

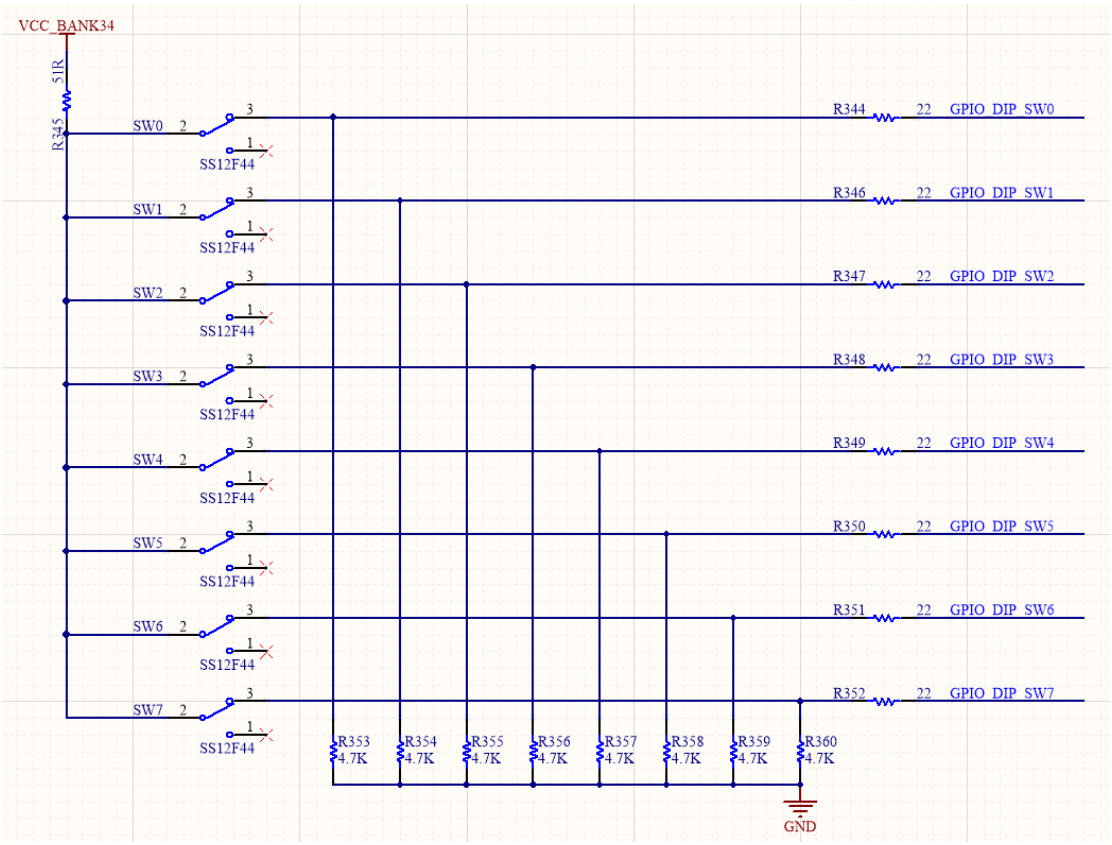


Figure 9.1 Schematics of Toggle Switches

Figure 9.2 Toggle Switches Physical Picture

Toggle switches pin assignment

Signal Name	FPGA Pin
SW0	N8
SW1	M5
SW2	P4
SW3	N4
SW4	U6
SW5	U5
SW6	R8
SW7	P8

10）LED

The development board has eight LEDs. When the pin is low, the LED emits light, and when it is high, the LED does not emit light. The schematic is shown in Figure 10.1.

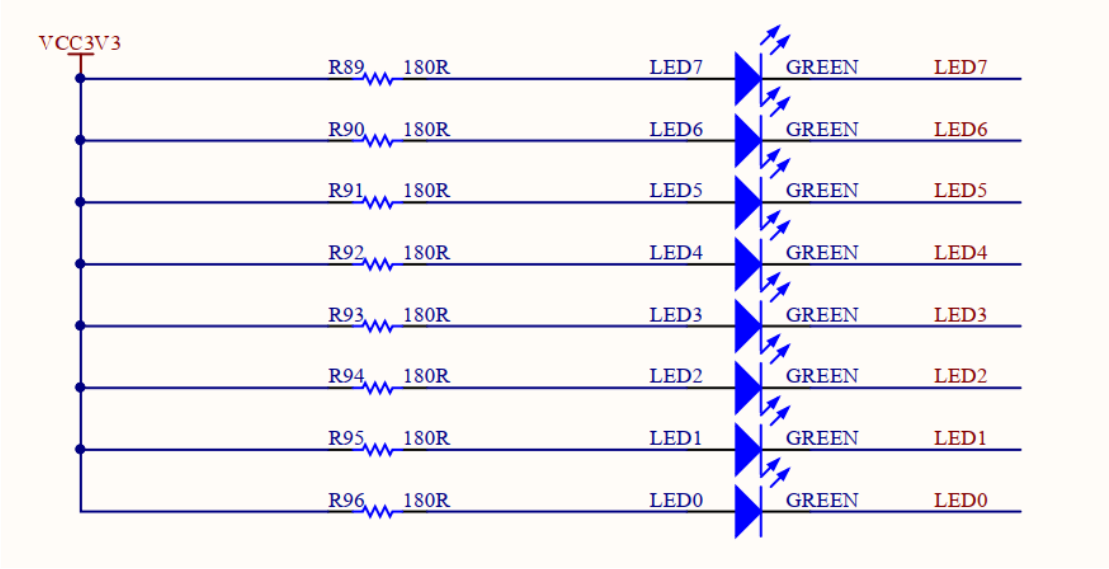


Figure 10.1 Schematics of LED

Figure 10.2 LED Physical Picture

LED pin assignment

Signal Name	FPGA Pin
LED0	N17
LED1	M19
LED2	P16
LED3	N16
LED4	N19
LED5	P19
LED6	N24
LED7	N23

11）Configuration Chip FLASH

The N25Q128A is a serial FLASH chip with a capacity of 128Mbit, which is more than enough for storing programs in the FPGA. Figure 11.1 shows the N25Q128A in the schematics.

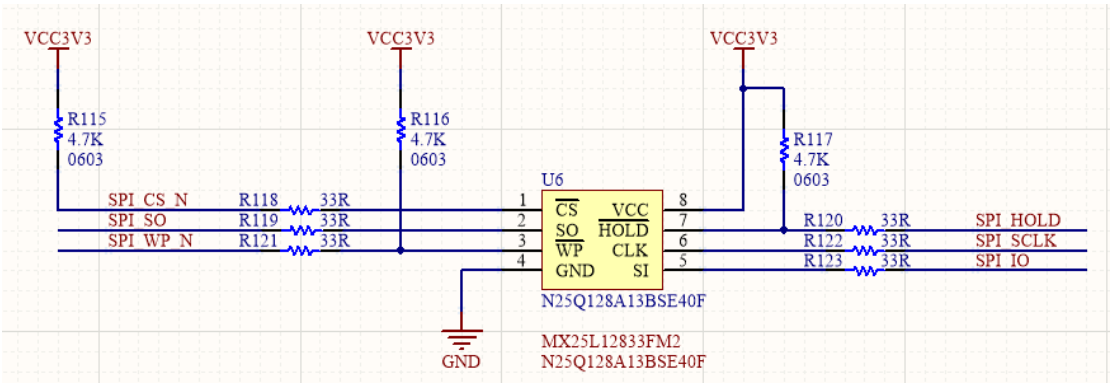


Figure 11.1 Schematics of FLASH

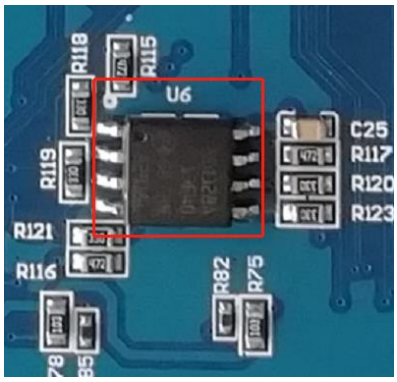


Figure 11.2 FLASH Physical Picture

12）GPIO（PMOD）Expansion Interface

The development board has four GPIO interfaces and is also a standard PMOD interface. The P1 and P2 interfaces each contain 6 standard IO pins of PFGA resources, 2 GND signals, and 2 adjustable power signals. The P3 and P4 interfaces

contain 4 pairs of LVDS signals, which can also be used as 8 standard IOs; 2 GND signals, and 2 adjustable power signals. It can be used with the BD5640-PMOD camera sub-board or the BD9226 high-speed AD sub-board. The daughter boards are available at the official online store. The schematics is as follows:

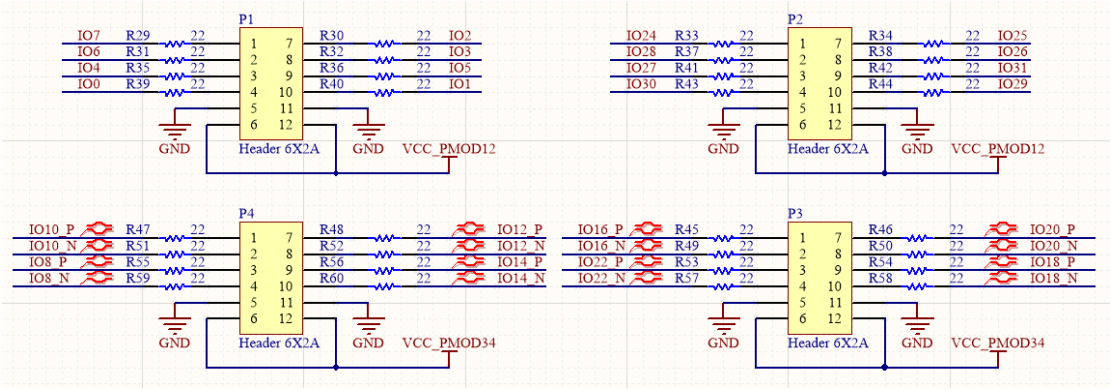


Figure 12.1 Schematics of GPIO

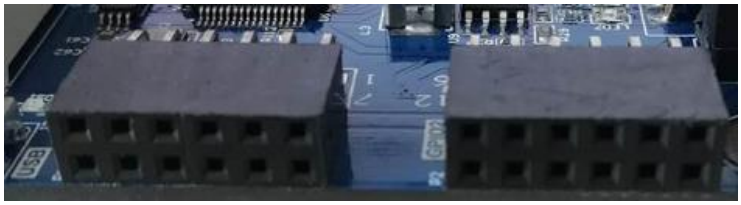


Figure 12.2 GPIO Physical Picture

Figure 12.3 GPIO Interface with BD5640 Camera Daughter Board

Figure 12.4 GPIO Interface with BD9226 High-speed AD Daughter Board

GPIO pin assignment

Signal Name	FPGA Pin	Description
P1-1	V21	Standard IO
P1-2	V22	Standard IO
P1-3	V23	Standard IO
P1-4	U24	Standard IO
P1-5		GND
P1-6		VCC-jumper J18
P1-7	AA22	Standard IO
P1-8	AA23	Standard IO
P1-9	W23	Standard IO
P1-10	V24	Standard IO
P1-11		GND
P1-12		VCC-jumper J18
P2-1	U19	Standard IO
P2-2	U14	Standard IO
P2-3	U16	Standard IO
P2-4	V16	Standard IO
P2-5		GND
P2-6		VCC-jumper J18
P2-7	T15	Standard IO
P2-8	U15	Standard IO
P2-9	V17	Standard IO
P2-10	V14	Standard IO

P2-11		GND
P2-12		VCC-jumper J18
P3-1	J6	LVDS1-P
P3-2	J5	LVDS1-N
P3-3	K7	LVDS2-P
P3-4	K6	LVDS2-N
P3-5		GND
P3-6		VCC-jumper J19
P3-7	L8	LVDS3-P
P3-8	K8	LVDS3-N
P3-9	G5	LVDS4-P
P3-10	F5	LVDS4-N
P3-11		GND
P3-12		VCC-jumper J19
P4-1	H8	LVDS5-P
P4-2	G8	LVDS5-N
P4-3	E6	LVDS6-P
P4-4	D6	LVDS6-N
P4-5		GND
P4-6		VCC-jumper J19
P4-7	H7	LVDS7-P
P4-8	G7	LVDS7-N
P4-9	F8	LVDS8-P
P4-10	F7	LVDS8-N
P4-11		GND
P4-12		VCC-jumper J19

13）JTAG Interface

The development board provides two JTAG interfaces, two programming download modes, which are selected by an SN74CBTLV3257 multiplexer when

downloading the FPGA program. The selection pin of the SN74CBTLV3257 is connected to the J6 jumper. The JTAG schematics is shown in Figure 13.1:

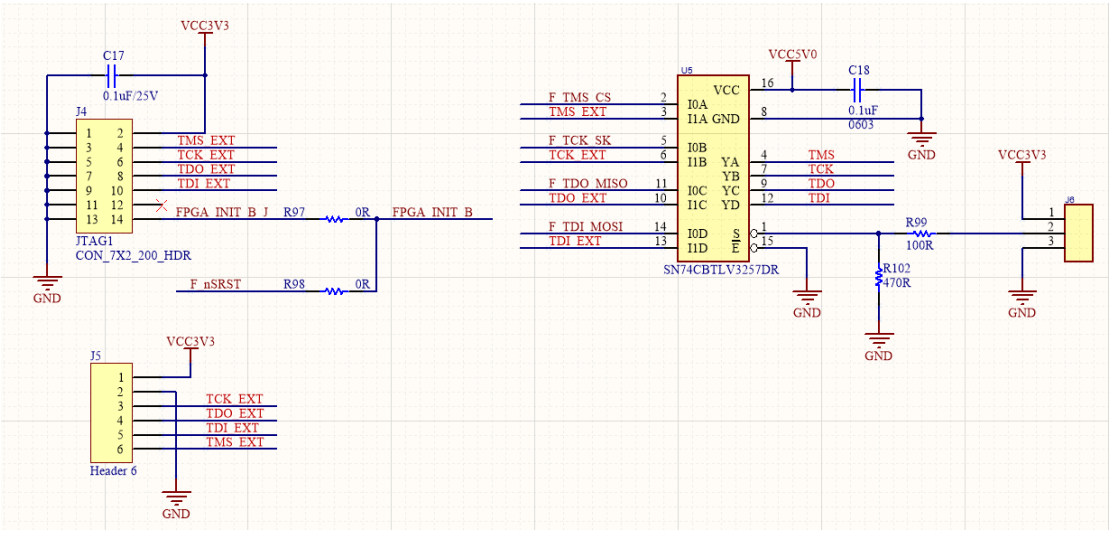


Figure 13.1 Schematics of JTAG Interface

Figure 13.2 JTAG Interface Physical Picture

JTAG pin assignment

Signal Name	FPGA Pin
TCK	H12(TCK)
GND	
TDO	J10(TDO)
VCC	
TMS	H11(TMS)
TDI	H10(TDI)

The second JTAG interface is "CPU_TAG", which downloads the program for the RISC-V CPU. The physical picture and pin assignments are as follows:

Figure 13.3 RISC-V Download Interface Physical Picture

RISC-V download interface pin assignment

Signal Name	FPGA Pin
CPU_TTDO	L24
CPU_TSRST_n	L25
CPU_TRST_n	M24
CPU_TRTCK	M25
CPU_TTDI	L22
CPU_TTMS	L23
CPU_TTCK	M21

14）UART Interface

A USB-B interface and a CP2102 chip are onboard for serial data communication.

The CP2102 features a high level of integration with a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) to support modem full-featured signals without the need for any external USB devices. Its characteristics are as follows

- Integrated USB transceiver; no external resistors required
- Integrated clock; no external oscillator required
- On-chip power-on reset circuit
- On-chip voltage regulator can output 3.3V voltage

- USB Specification 2.0 compliant
- USB suspend states supported via SUSPEND pins
- Asynchronous serial data bus is compatible with all handshake and modulation regulator interface signals
- Supported data formats are data bit 8, stop bit 1, 2 and check digit
- Intrinsic more than 512-byte receive buffer and 512-byte transmit buffer
- Hardware or X-On/X-Off handshaking supported

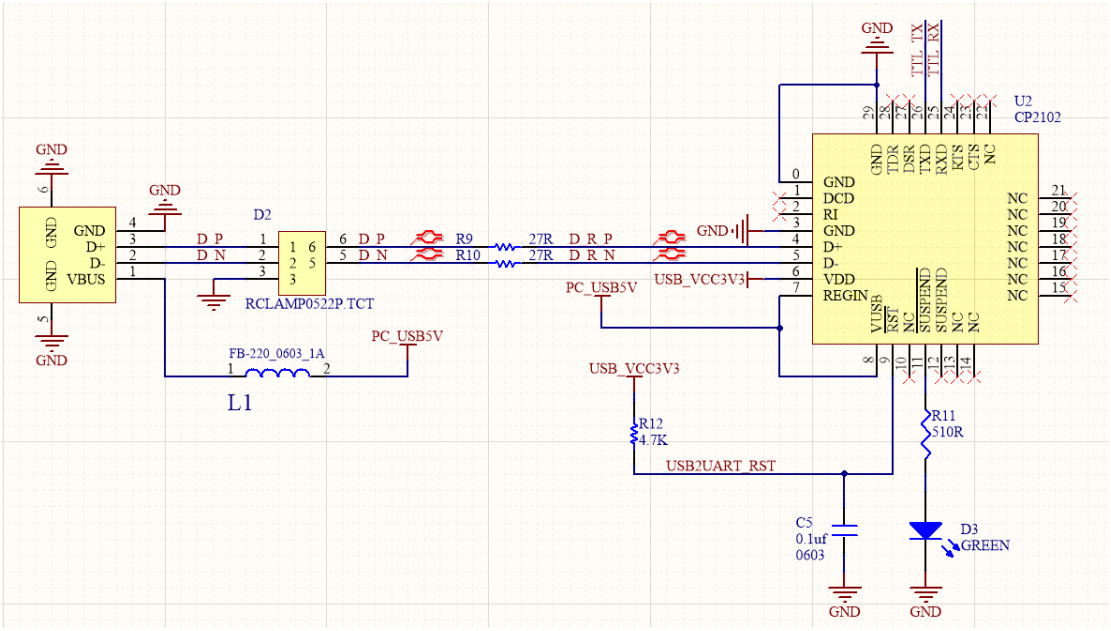


Figure 14.1 UART Schematics

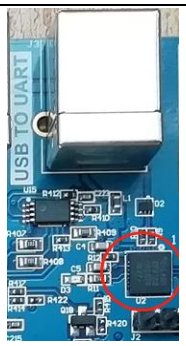


Figure 14.2 USB-B Interface and CP2102 Chip Physical Picture

UART pin assignment

Signal Name	FPGA Pin
TX	L17
RX	L18

15）SRAM

SRAM (Static Random-Access Memory) is a type of random-access memory. The "static" means that if the memory is kept energized, the data stored therein can be kept constant. In contrast, data stored in dynamic random-access memory (DRAM) needs to be updated periodically. However, when the power supply is stopped, the data stored in the SRAM will disappear (called volatile memory), which is different from the ROM or flash memory that can store data after the power is turned off. The development board has two Super SRAMs, which are connected in parallel to a 32-bit data interface. The maximum access space is up to 2M bytes, IS61WV51216 (2 pieces) 512K x 32bit. The design schematics is as follows:

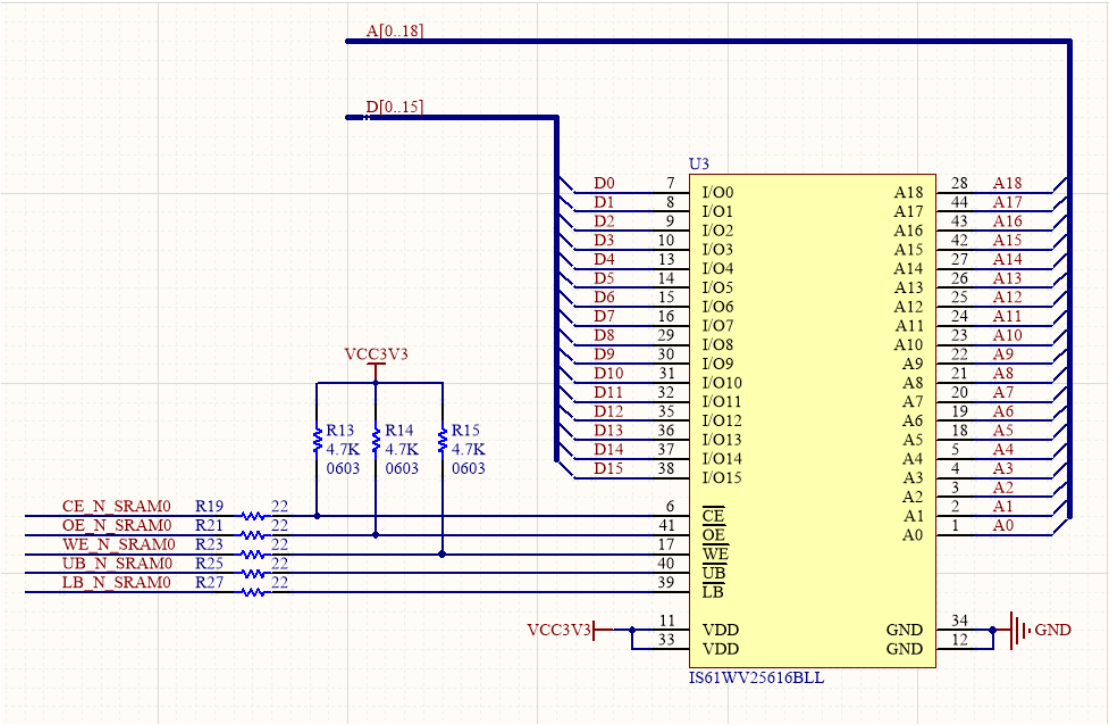


Figure 15.1 Schematics of SRAM0

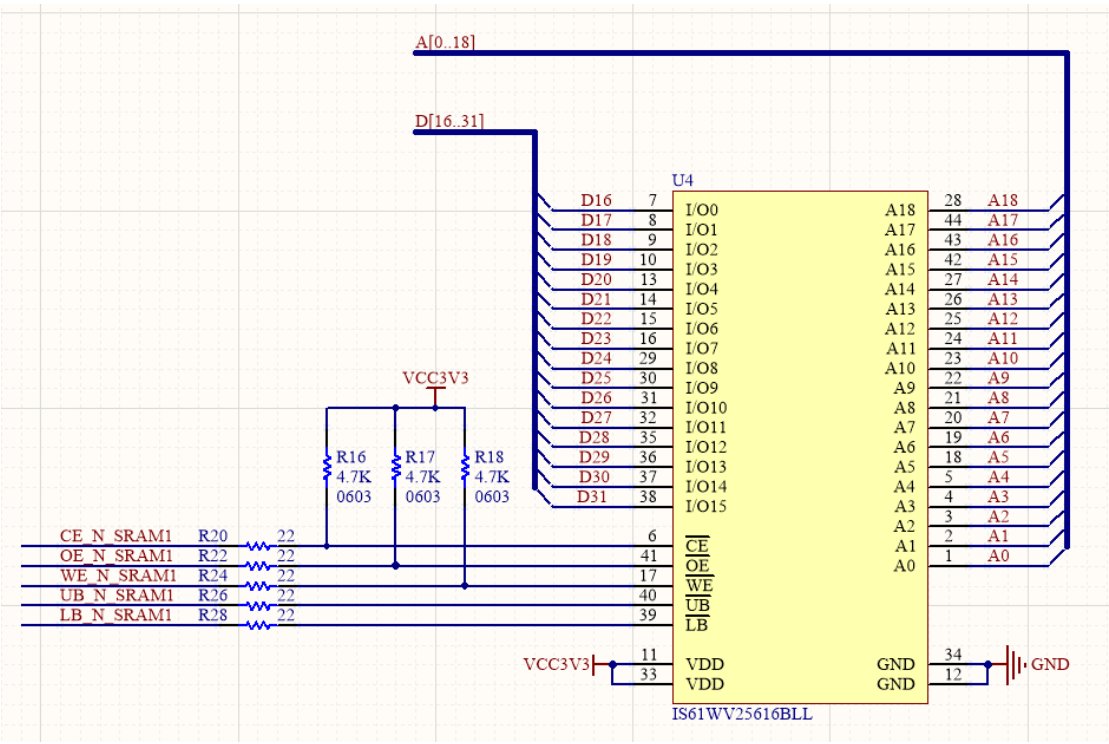


Figure 15.2 Schematics of SRAM1

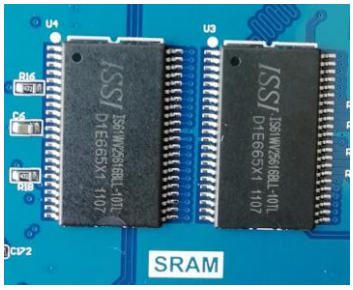


Figure 15.3 SRAM Physical Picture

SRAM pin assignment

Signal Name	FPGA Pin
SRAM0_CE_N	F25
SRAM0_OE_N	H23
SRAM0_WE_N	L19
SRAM0_UB_N	H24
SRAM0_LB_N	G26
SRAM0_IO0	U21
SRAM0_IO1	U25
SRAM0_IO2	W26
SRAM0_IO3	Y26
SRAM0_IO4	AA25
SRAM0_IO5	AB26
SRAM0_IO6	AA24
SRAM0_IO7	AB24
SRAM0_IO8	AC24
SRAM0_IO9	AC26
SRAM0_IO10	AB25
SRAM0_IO11	Y23
SRAM0_IO12	Y25
SRAM0_IO13	W25
SRAM0_IO14	V26
SRAM0_IO15	U26
SRAM0_A0/SRAM1_A0	E26

SRAM0_A1/SRAM1_A1	E25
SRAM0_A2/SRAM1_A2	D26
SRAM0_A3/SRAM1_A3	D25
SRAM0_A4/SRAM1_A4	G22
SRAM0_A5/SRAM1_A5	H18
SRAM0_A6/SRAM1_A6	M15
SRAM0_A7/SRAM1_A7	M16
SRAM0_A8/SRAM1_A8	L15
SRAM0_A9/SRAM1_A9	K23
SRAM0_A10/SRAM1_A10	J25
SRAM0_A11/SRAM1_A11	K22
SRAM0_A12/SRAM1_A12	H26
SRAM0_A13/SRAM1_A13	J26
SRAM0_A14/SRAM1_A14	J24
SRAM0_A15/SRAM1_A15	G25
SRAM0_A16/SRAM1_A16	G24
SRAM0_A17/SRAM1_A17	J21
SRAM0_A18/SRAM1_A18	J23
CE_N_SRAM1	E23
OE_N_SRAM1	F23
WE_N_SRAM1	J18
UB_N_SRAM1	F24
LB_N_SRAM1	K20
SRAM1_IO0	T14
SRAM1_IO1	T17
SRAM1_IO2	W18
SRAM1_IO3	U17
SRAM1_IO4	V18
SRAM1_IO5	T18
SRAM1_IO6	W19
SRAM1_IO7	T19

SRAM1_IO8	W21
SRAM1_IO9	Y22
SRAM1_IO10	Y21
SRAM1_IO11	U20
SRAM1_IO12	T20
SRAM1_IO13	W20
SRAM1_IO14	Y20
SRAM1_IO15	V19

16）Audio

There is a piece WM8978 onboard, which is a stereo multimedia digital signal codec with speaker driver. The WM8978 is a low power, high quality stereo multimedia digital signal codec. It is mainly used in portable applications such as digital cameras and portable digital camcorders. It combines stereo differential microphone preamplifiers with speakers, headphones and differential, stereo line output drivers to reduce the external components necessary for the application, such as advanced on-chip digital signal processing function with separate microphone or headphone amplifiers, including a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. The WM8978 digital audio interface can operate as a master or a slave. An internal PLL can generate all required audio clocks for the CODEC from common reference clock frequencies. The design schematic is as follows

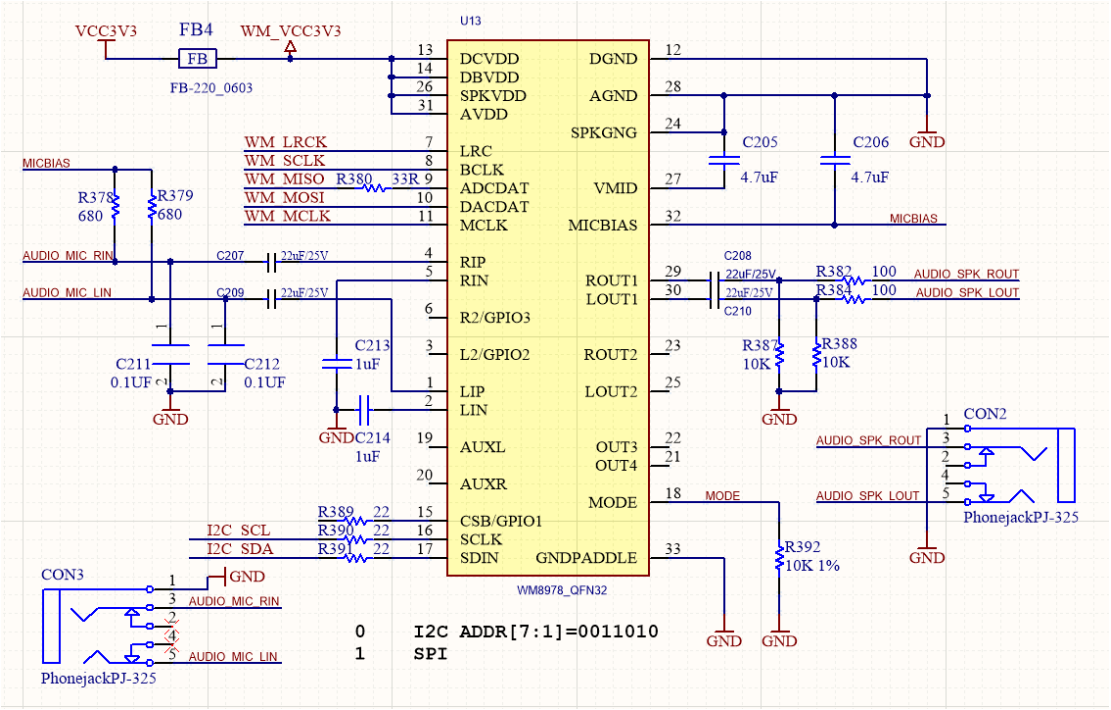


Figure 16.1 Schematics of Audio

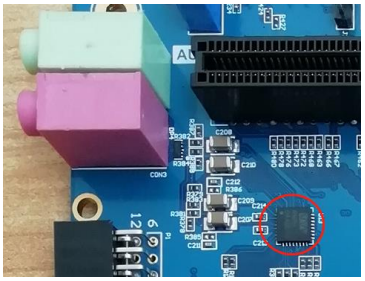


Figure 16.2 Audio Interface and Chip Physical Picture

Pin assignment

Signal Name	FPGA Pin
WM_LRC	H15
WM_BCLK	F18
WM_ADCDAT	G19
WM_DACDAT	F20
WM_MCLK	H17
WM_SCLK	R20
WM_SDIN	R21

17）USB Keyboard and Mouse Interface

CH9350L is a USB keyboard and mouse to serial communication control chip. Combined with the simple and easy-to-use features of the asynchronous serial port, the USB communication mode between the USB keyboard, the mouse and the FPGA are extended to the asynchronous serial port (UART), which facilitates data integration with audio, video and other signals.

CH9350L features:

- Support 12Mbps full speed USB transmission and 1.5Mbps low speed USB transmission, compatible with USBV2.0
- The upper-end USB port complies with the standard HD-type protocol and does not require additional driver installation. It supports Windows, Linux, MAG and other operating systems with built-in HD device drivers.
- The same chip can be configured as the host computer mode and the client computer mode, respectively connected to USB-Host and USB keyboard and mouse in the same mode to configure different working states, suitable for a variety of applications.
- Support USB keyboard and mouse in the BIOS interface, support multimedia function keys, support different resolution USB mouse
- Support various brands of USB keyboard and mouse, USB wireless keyboard and mouse, USB to PS2 line, USB scanner, etc.
- The host and client terminals support hot swap
- Provides a transmit status pin to support 485 communication
- The serial port supports the 300000/115200/57600/38400 serial

communication baud rate.

- Built-in oscillator and power-on reset circuit, the peripheral circuit is simple.
- Support 5V, 3.3V power supply voltage

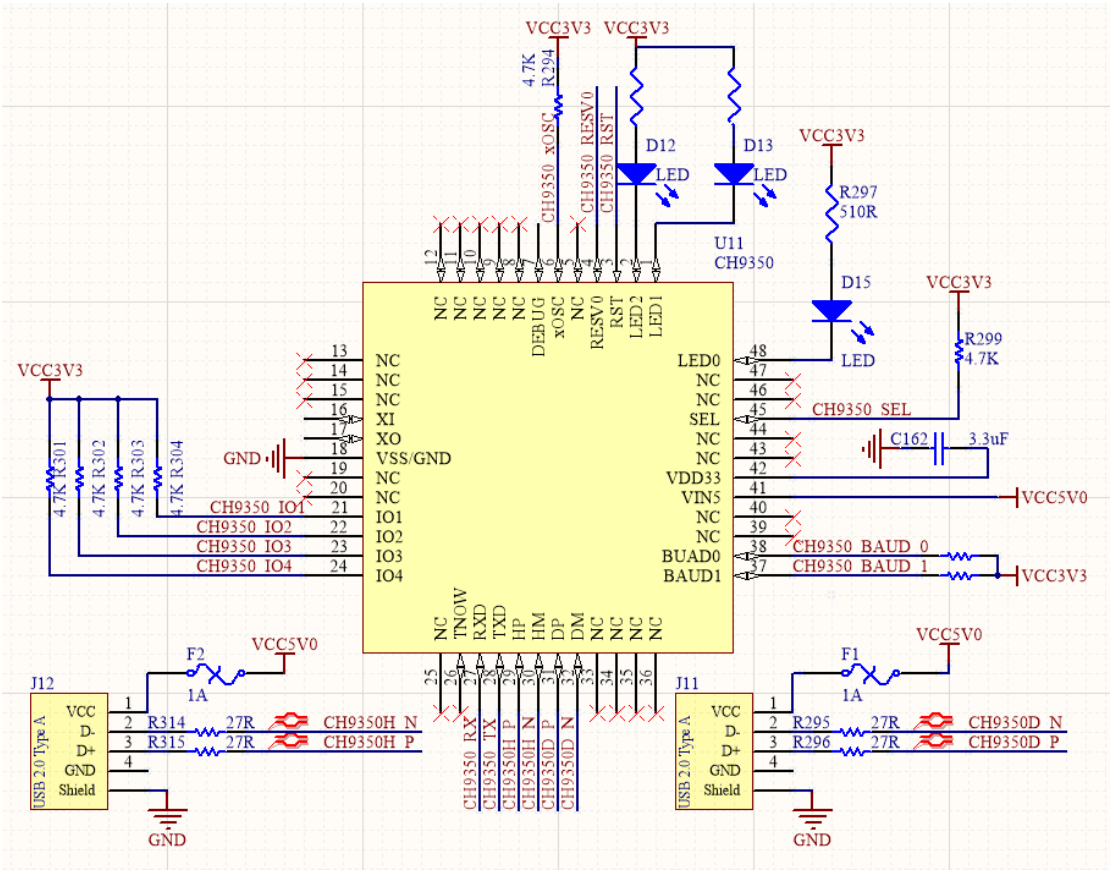


Figure 17.1 Schematics of USB Keyboard and Mouse

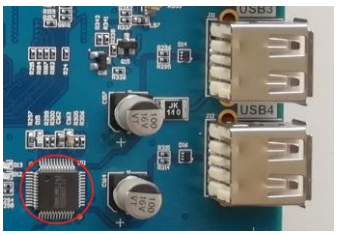


Figure 17.2 USB Interface Physical Picture

Pin assignment

Signal Name	FPGA Pin
CH9350_RST	M17
CH9350_RXD	H21
CH9350_TXD	H22

18）TFT LCD Interface

The development board reserves a TFTLCD touch display interface, and the signal is connected. Adaptable to 3.5 inches touch LCD module TFT LCD screen 320X480. Interface and matching LCD screen (LCD screen available in official online store), as shown below:

Figure 18.1 LCD Interface Physical Picture

Figure 18.2 3.5” LCD Touch Display

Pin assignment

Signal Name	FPGA Pin	Description
Pin 1	H14	CS
Pin 2	B26	RS
Pin 3	D24	WR
Pin 4	C26	RD
Pin 5	E21	RST

Pin 6	U21	DB0
Pin 7	U25	DB1
Pin 8	W26	DB2
Pin 9	Y26	DB3
Pin 10	AA25	DB4
Pin 11	AB26	DB5
Pin 12	AA24	DB6
Pin 13	AB24	DB7
Pin 14	AC24	DB8
Pin 15	AC26	DB9
Pin 16	AB25	DB10
Pin 17	Y23	DB11
Pin 18	Y25	DB12
Pin 19	W25	DB13
Pin 20	V26	DB14
Pin 21	U26	DB15
Pin 22		GND
Pin 23	T14	BL
Pin 24		VCC3V3
Pin 25		VDD3V3
Pin 26		GND
Pin 27		GND
Pin 28		BL_VDD
Pin 29	T17	MISO
Pin 30	W18	T_MOSI
Pin 31	U17	T_PEN
Pin 32	V18	T_BUSY
Pin 33	G15	T_CS
Pin 34	W19	T_CLK
Pin 35		G_PAD
Pin 36		G_PAD

19）40-pin Extended GPIO Interface

Figure 19.1 Extended GPIO Interface Physical Picture

Pin assignment

Signal Name	FPGA Pin	Description
Pin 1	H9	GPIO_0
Pin 2	J8	GPIO_1
Pin 3	A5	GPIO_2
Pin 4	G9	GPIO_3
Pin 5	B5	GPIO_4
Pin 6	A4	GPIO_5
Pin 7	A3	GPIO_6
Pin 8	B4	GPIO_7
Pin 9	B2	GPIO_8
Pin 10	A2	GPIO_9
Pin 11	F4	GPIO_10
Pin 12	D5	GPIO_11
Pin 13	G6	GPIO_12
Pin 14	C4	GPIO_13
Pin 15	H4	GPIO_14
Pin 16	D4	GPIO_15
Pin 17	J4	GPIO_16
Pin 18	E3	GPIO_17
Pin 19	E5	GPIO_18
Pin 20	C2	GPIO_19

Pin 21	D3	GPIO_20
Pin 22	C3	GPIO_21
Pin 23	H6	GPIO_22
Pin 24	B1	GPIO_23
Pin 25	F3	GPIO_24
Pin 26	C1	GPIO_25
Pin 27	D1	GPIO_26
Pin 28	E2	GPIO_27
Pin 29	F2	GPIO_28
Pin 30	E1	GPIO_29
Pin 31	G4	GPIO_30
Pin 32	G2	GPIO_31
Pin 33	G1	GPIO_32
Pin 34	H3	GPIO_33
Pin 35	K7	IO22_P
Pin 36	K6	IO22_N
Pin 37		GND
Pin 38		GND
Pin 39		VCC3V3
Pin 40		VCC3V3

20) High Speed Bus Connector

PCI-Express (Peripheral Component Interconnect Express) connector is used here. It is not related to the PCIE bus standard. The main advantage is the high data transfer rate. The onboard PCIE connector can be used with the BD5640 camera daughter board, which is available at the official online store.

Figure 20.1 PCIE Interface Physical Picture

Figure 20.2 BD5640 Daughter Board

Pin assignment

Signal Name	FPGA Pin	Description
A1		
A2		12V
A3		12V
A4		GND
A5	H2	JTAG2/TCK
A6	H1	JTAG3/TDI
A7	J3	JTAG4/TDO
A8	K3	JTAG5/TMS
A9		3.3V
A10		3.3V
A11		PERST
A12		GND
A13	N3	REFCLK+
A14	N2	REFCLK-
A15		GND
A16	M2	PERp0
A17	L2	PERn0
A18		GND
A19		RESERVED
A20		GND
A21	N7	PERp2

A22	N6	PERn2
A23		GND
A24	T5	GND
A25	R5	PERp3
A26		PERn3
A27		GND
A28		GND
A29	T4	PERp3
A30	T3	PERn3
A31		GND
A32	R6	RESERVED
B1		12V
B2		12V
B3		12V
B4		GND
B5	R3	SMCLK
B6	P3	SMDAT
B7		GND
B8		3.3V
B9	K2	JTAG1/TRST#
B10		3.3Vaux
B11		WAKE#
B12	L3	RESERVED
B13		GND
B14	K1	PETp0
B15	J1	PETn0
B16		GND
B17		PRSNT#2
B18		GND
B19	N1	PETp1
B20	M1	PETn1
B21		GND
B22		GND
B23	M7	PETp2
B24	L7	PETn2
B25		GND
B26		GND
B27	U2	PETp3
B28	U1	PETn3
B29		GND
B30	P5	RESERVED

B31	P6	PRSNT#2
B32		GND

3. References

1. https://www.nxp.com/docs/en/data-sheet/PCF8591.pdf
2. https://www.verical.com/datasheet/realtek-semiconductor-phy-rtl8211e-vb-cg-2635459.pdf#page=36&zoom=100,0,105
3. https://www.silabs.com/documents/public/data-sheets/CP2102-9.pdf
4. https://www.mouser.com/ds/2/76/WM8978_v4.5-1141768.pdf