

FII_PRA006-010_V1.0_R0.2

GPIO(PMOD X 2)

7-SEG DISPLAY x 6

LED X 8

USB 2 UART

AD/DA

**ALTERA
CYCLONE 10 LP
10CL006YE144C8G**

OSC_50M

BUTTON x 4

VGA

SWITCH x 8

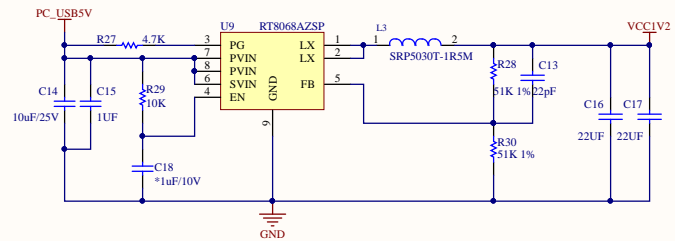
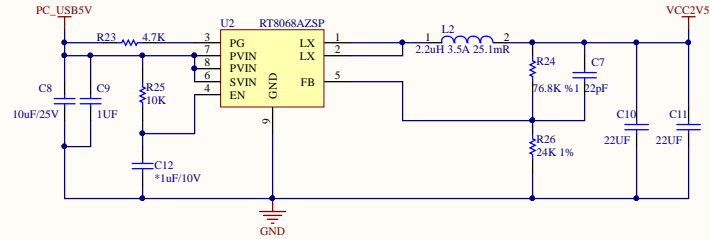
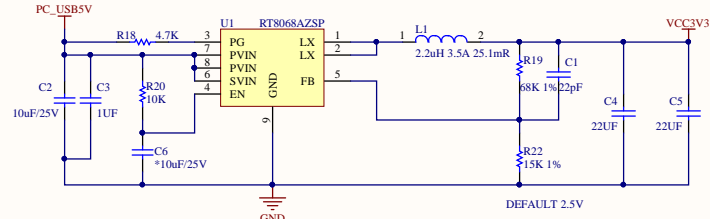
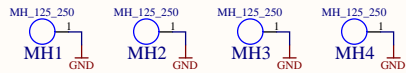
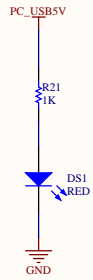
I2C EEPROM

ETHERNET(1G)

IIC Addressing	
8'B1010000X	IIC EEPROM
8'B1001000X	PCF8591T

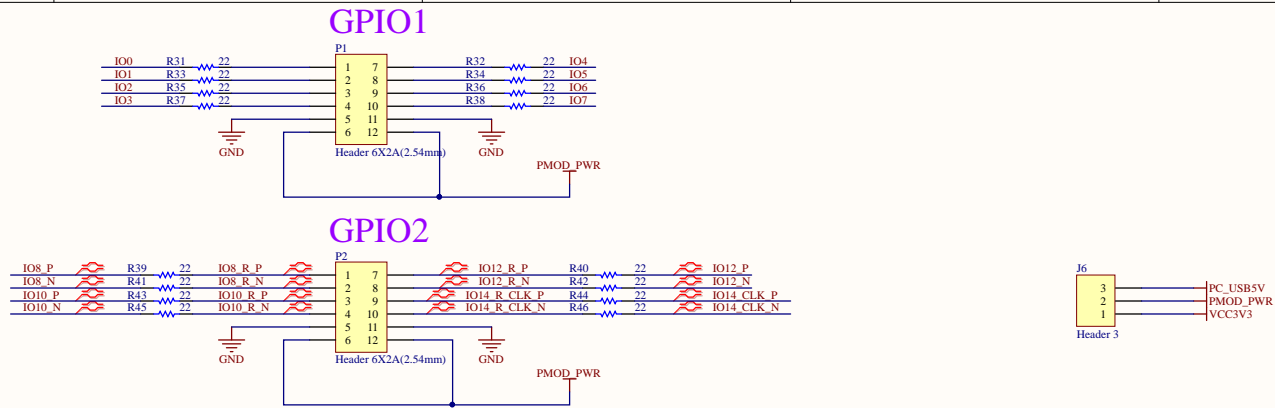
Company: FII		Title: Top_Diagram of PRA006	
Date: 2019-07-20	Time: 3:41:33 PM	Engineer: WG RJ	Size: A4
Revision: R3.0	Sheet 1 of 14		

Power

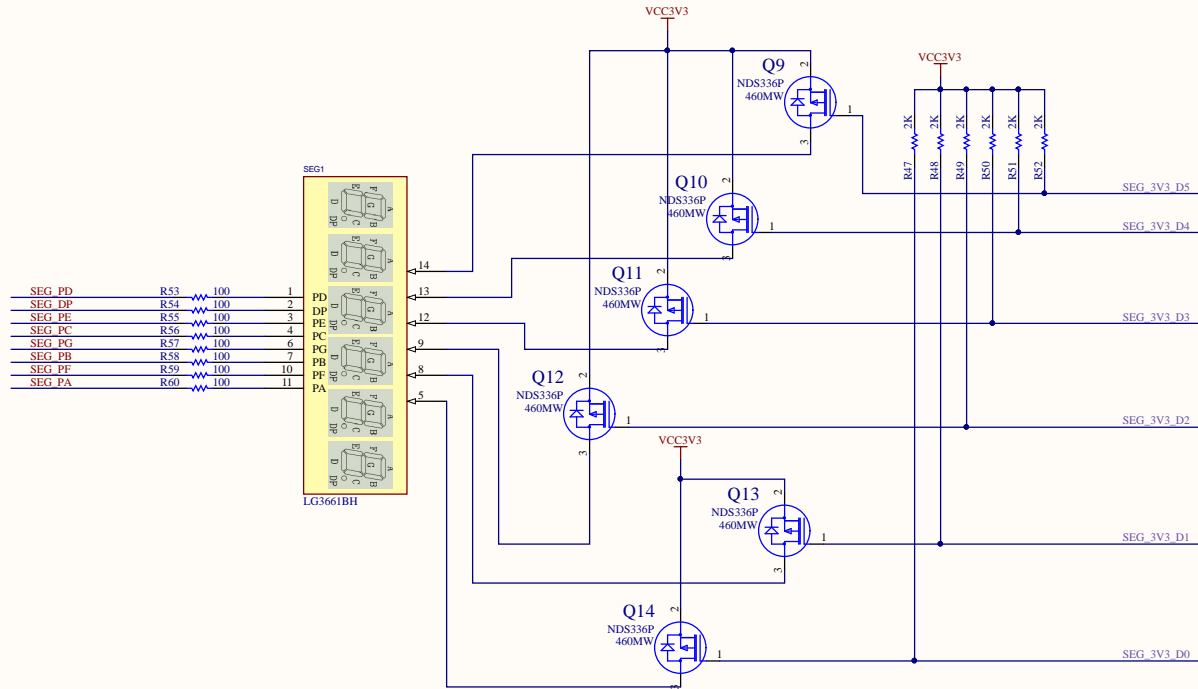


$$V_{out} = 0.6 \times (1 + R1/R2)$$

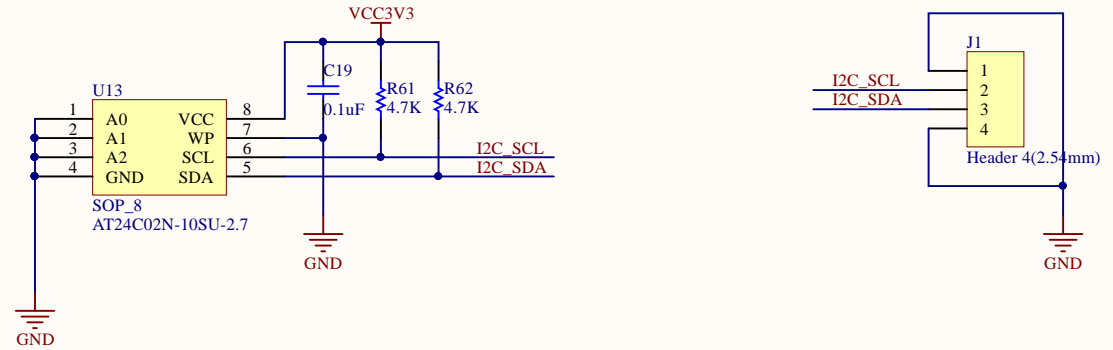
GPIO



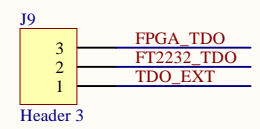
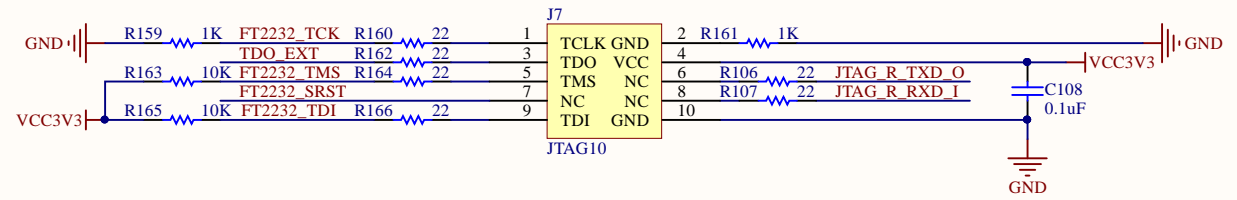
SEG



I2C

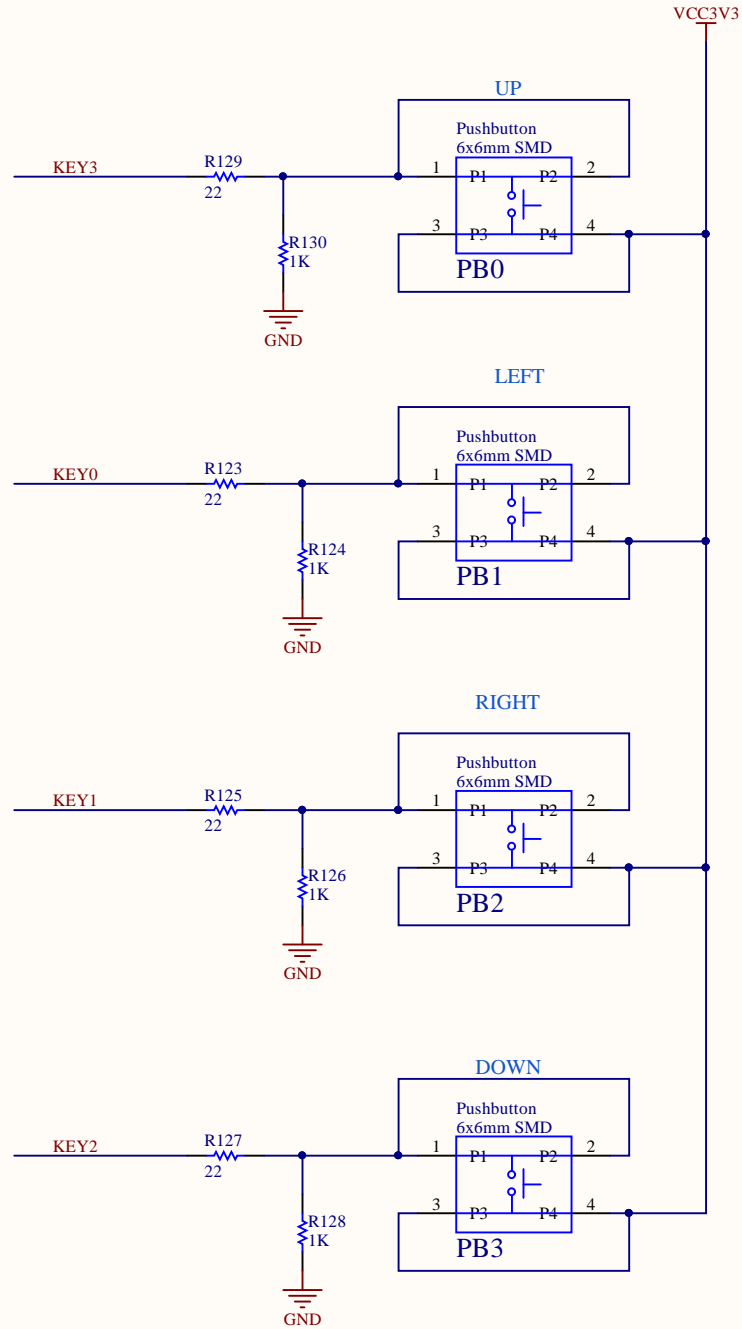


JTAG



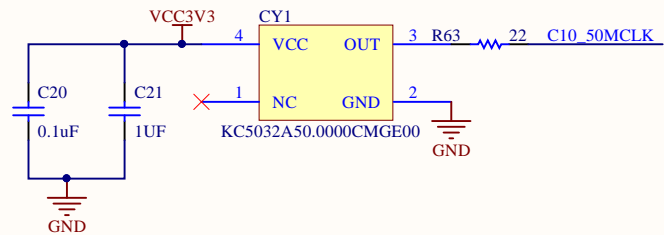
Company: FII		Title: I2C_EEPROM_JTAG of PRA006	
Date: 2019-07-20	Time 3:41:33 PM	Engineer: WG RJ	Size: A4
Revision: R3.0	Sheet 4 of 14		

KEYPAD

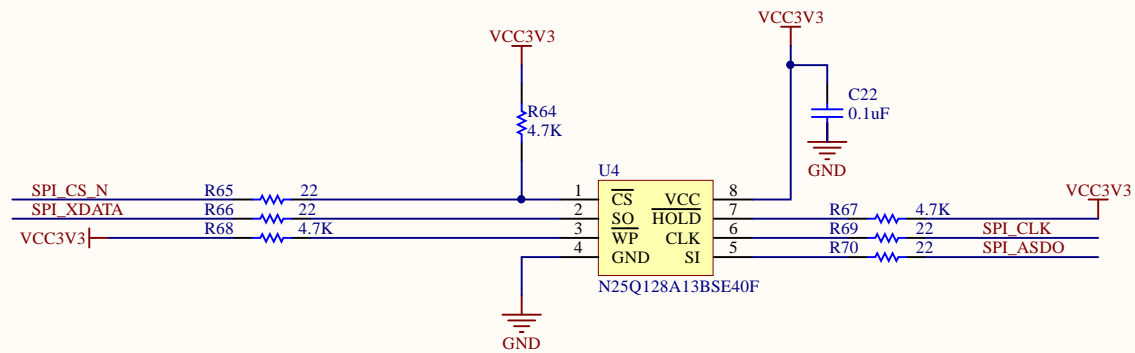


Company: FII	Title: BUTTON	of PRA006	
Date: 2019-07-20	Time 3:41:33 PM	Engineer: WG RJ	Size: A4
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XTAL

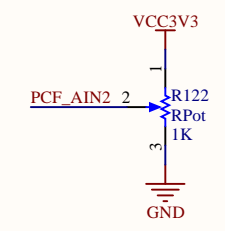
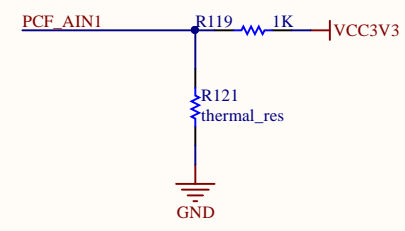
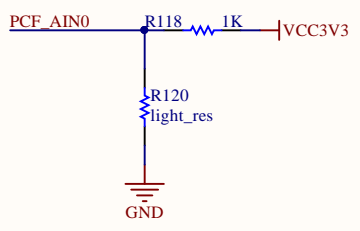
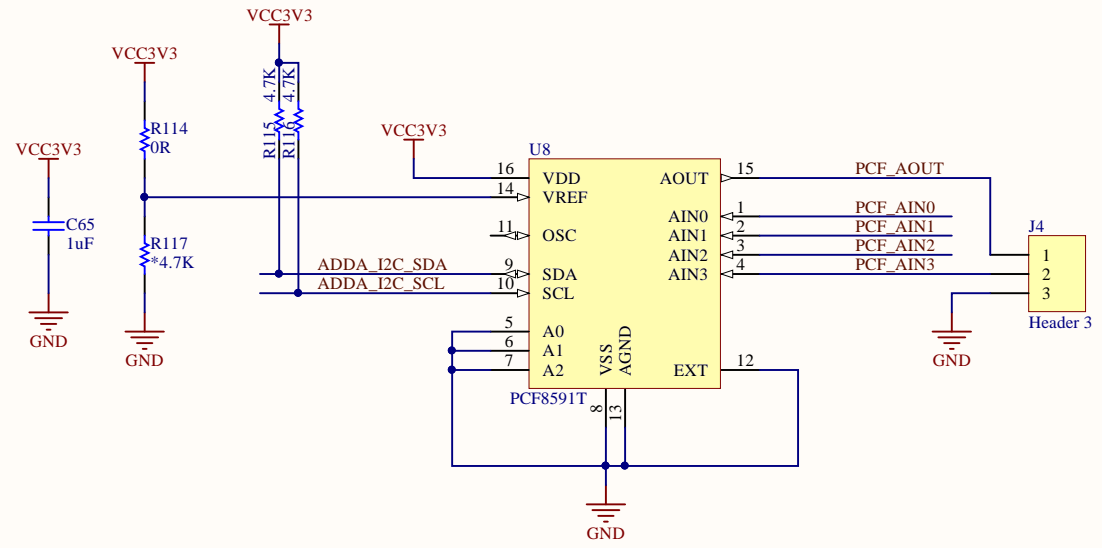


FLASH



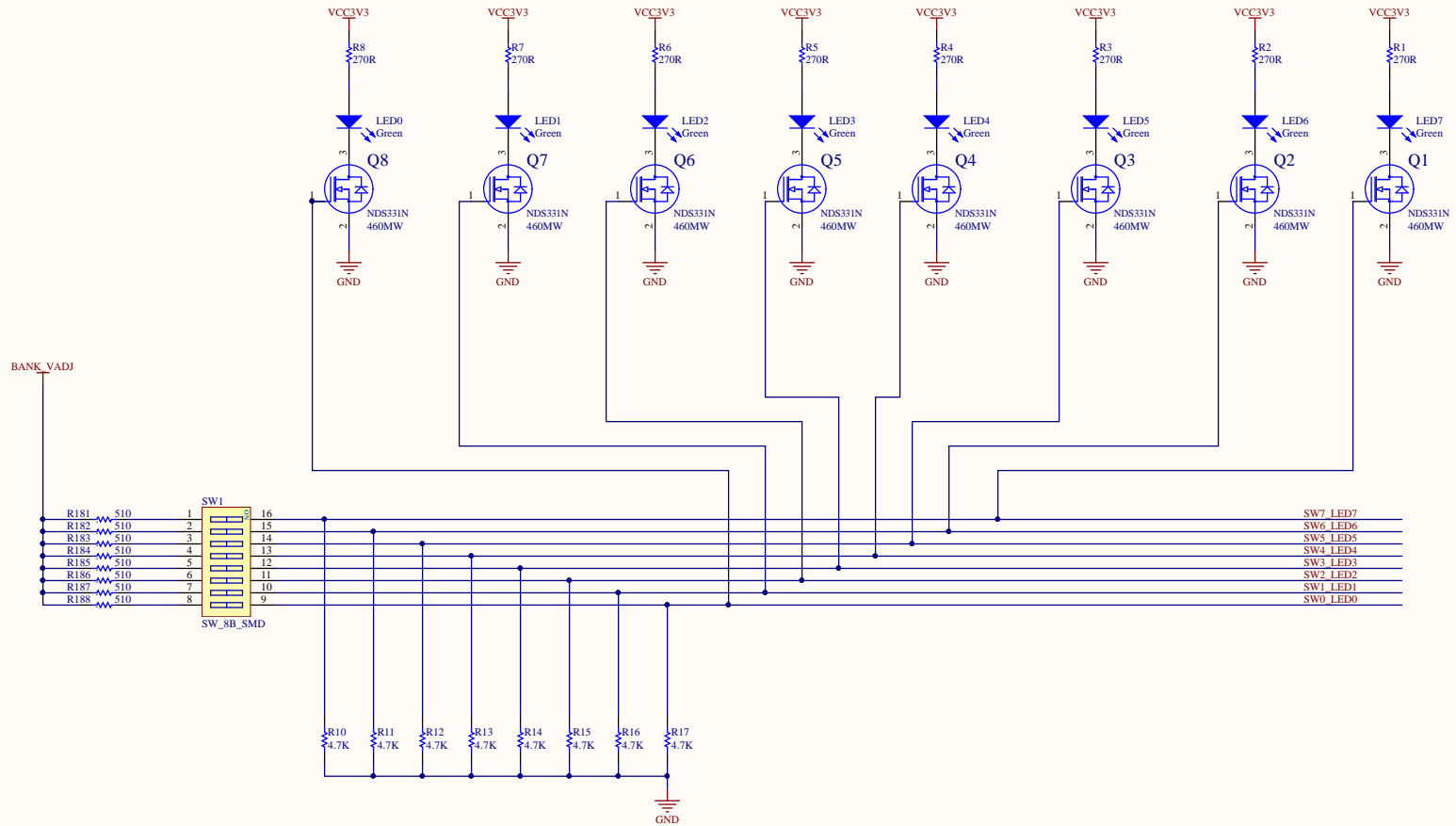
Company: FII	Title: OSC_FLASH of PRA006	
Date: 2019-07-20	Time 3:41:33 PM	Engineer: WG RJ
Revision: R3.0	Sheet 6 of 14	Size: A4

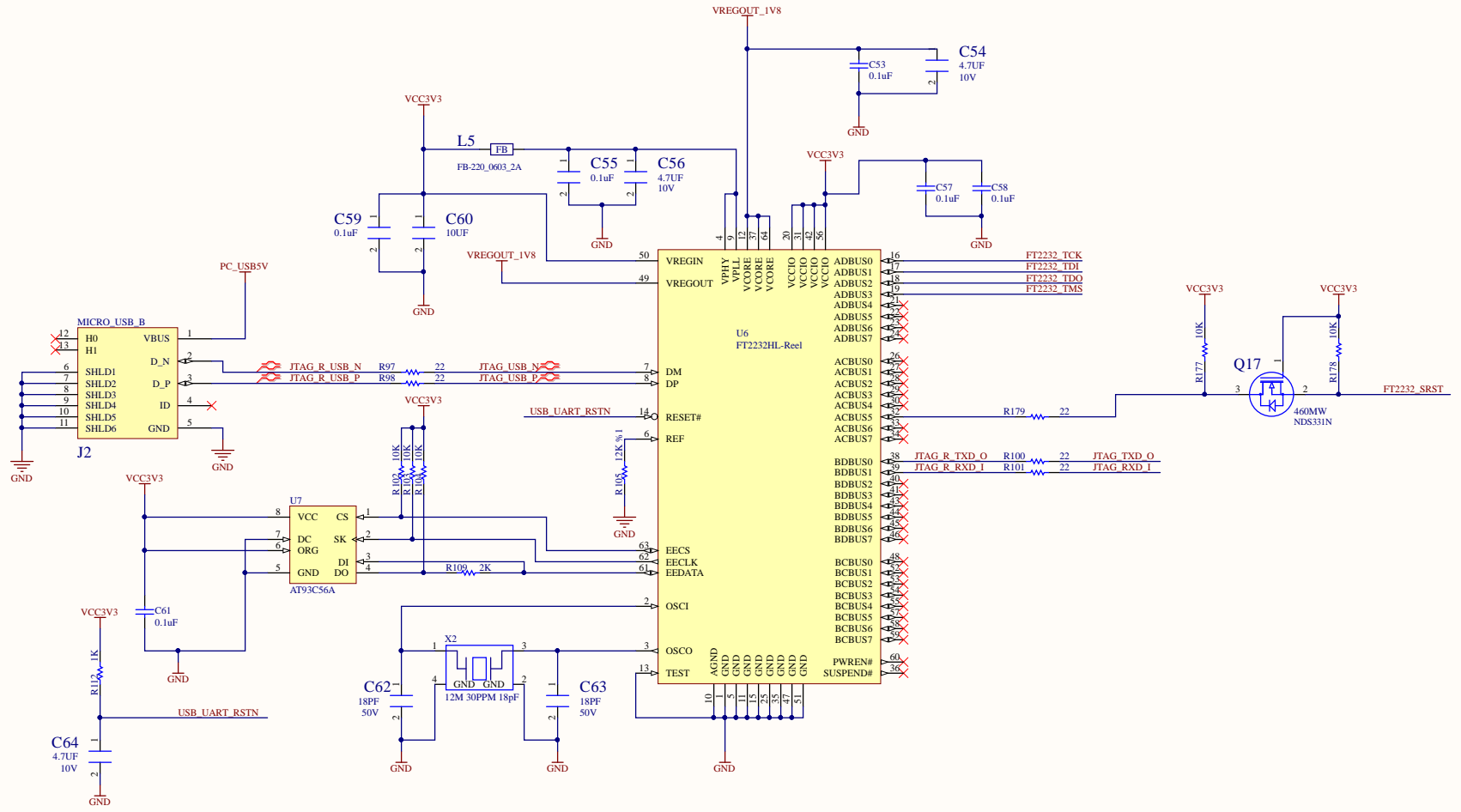
AD/DA



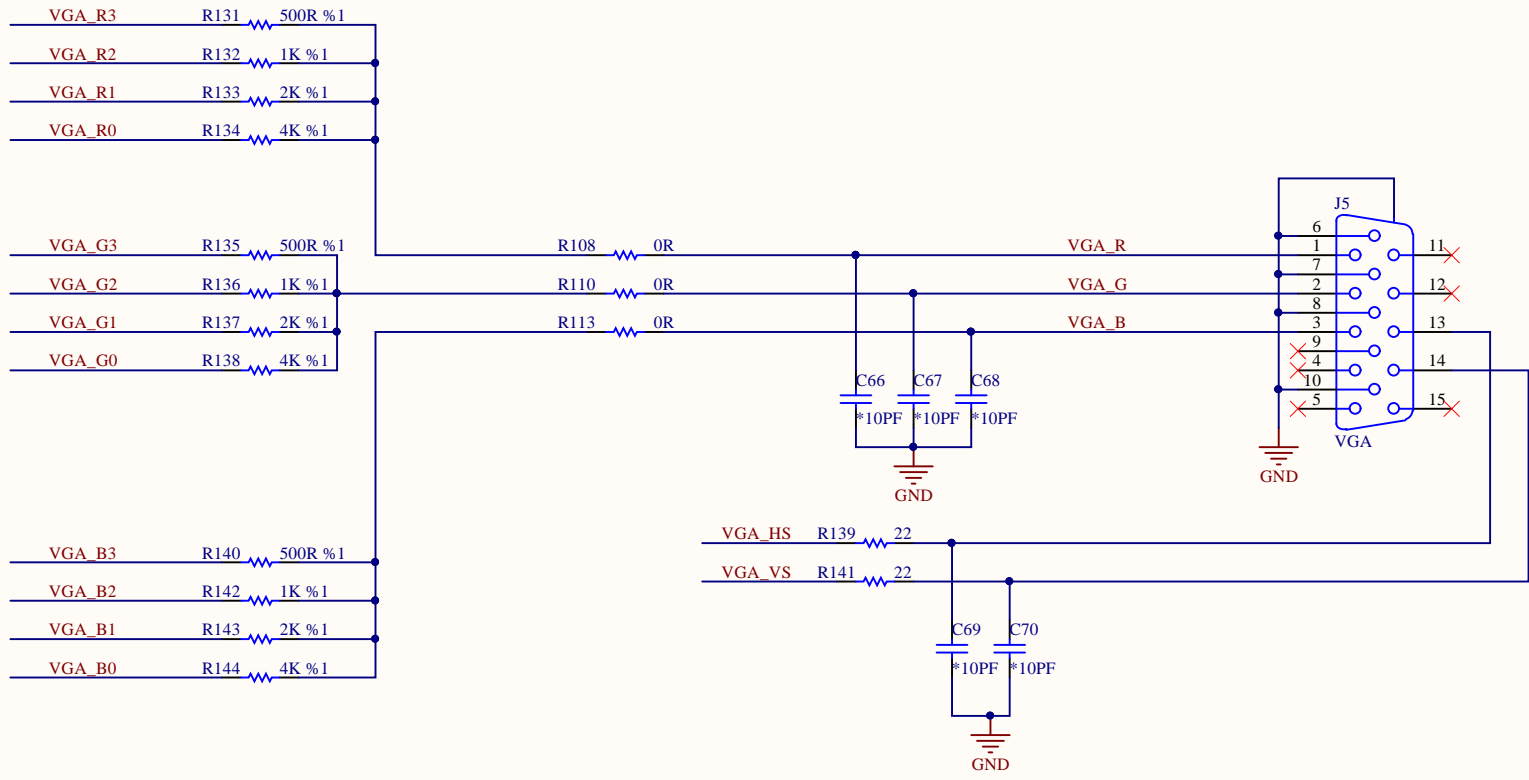
Company: FII		Title: AD_DA of PRA006	
Date: 2019-07-20	Time 3:41:33 PM	Engineer: WG RJ	Size: A4
Revision: R3.0	Sheet 7 of 14		

SWITCH LED

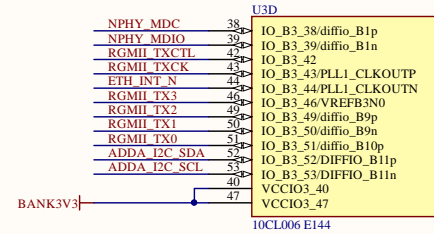
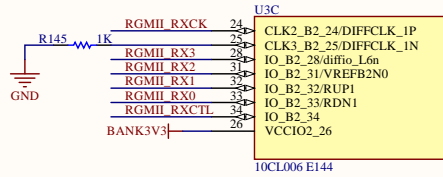
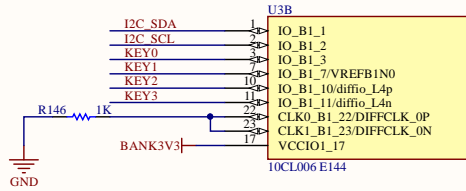




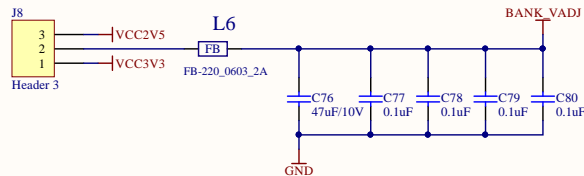
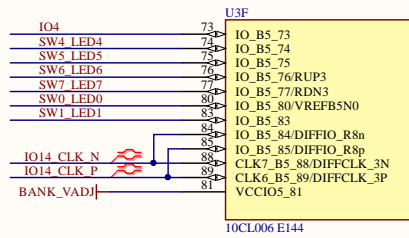
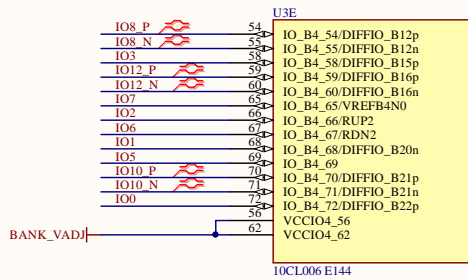
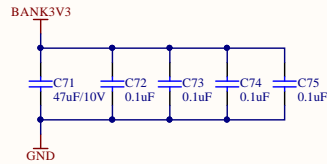
Company: FH	Title: USB_2_UART	of	PRA006
Date: 2019-07-20	Time 3:41:34 PM	Engineer: WG RJ	Size: B+
Revision: R3.0	Sheet 10	of 14	



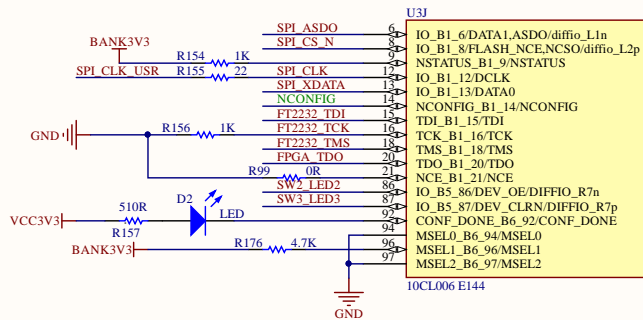
Company: FII		Title: VGA of PRA006	
Date: 2019-07-20	Time 3:41:34 PM	Engineer: WG RJ	Size: A4
Revision: R3.0	Sheet 11 of 14		



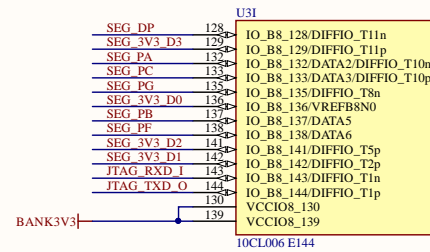
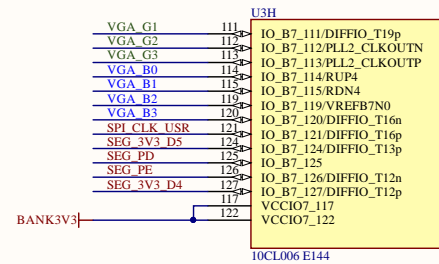
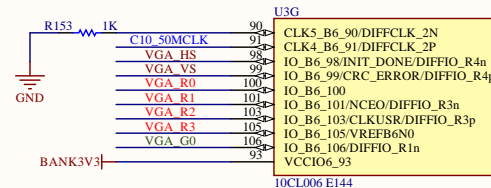
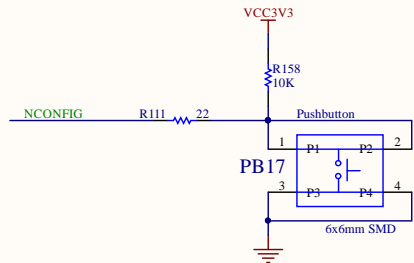
RGMII TX0	R147	22	RG0_TX0
RGMII TX1	R148	22	RG0_TX1
RGMII TX2	R149	22	RG0_TX2
RGMII TX3	R150	22	RG0_TX3
RGMII TXCTL	R151	22	RG0_TXCTL
RGMII TXCK	R152	22	RG0_TXCK

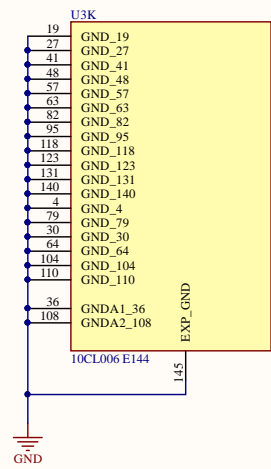
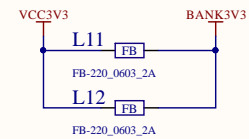
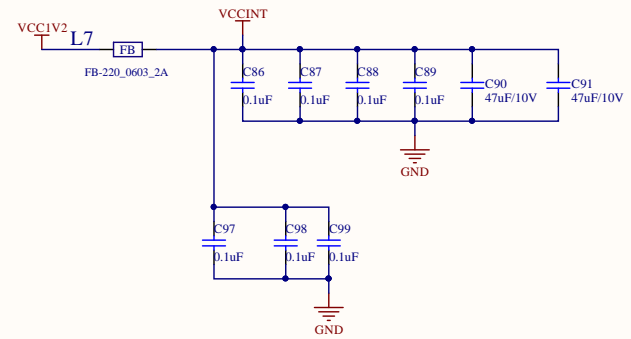
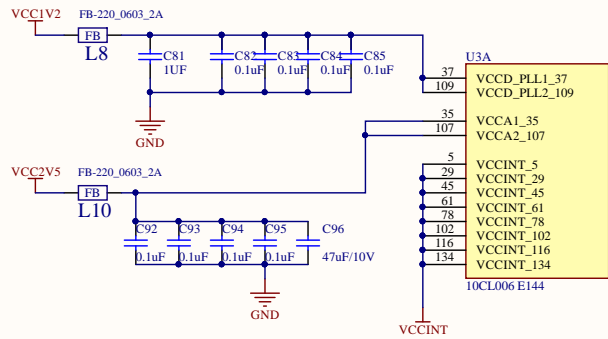


Company: FH	Title: FPGA_1	of PRA006
Date: 2019-07-20	Time 3:41:34 PM	Engineer: WG RJ
Revision: R3.0	Sheet 12 of 14	Size: B



Cannot open file MSEL_PIN_SETTING.PNG





Company: FH	Title: FPGA_POWER_GND of PRA006	
Date: 2019-07-20	Time 3:41:34 PM	Engineer: WG RJ
Revision: R3.0	Sheet 14 of 14	Size: B