FII-PRA040 Hardware Reference Guide

V1.1

FRASER INNOVATION INC

Version Control

version	Date	Description
1.0	07/17/2019	Initial Release
1.1	07/19/2019	Add Oscillator Part

Copyright Notice:

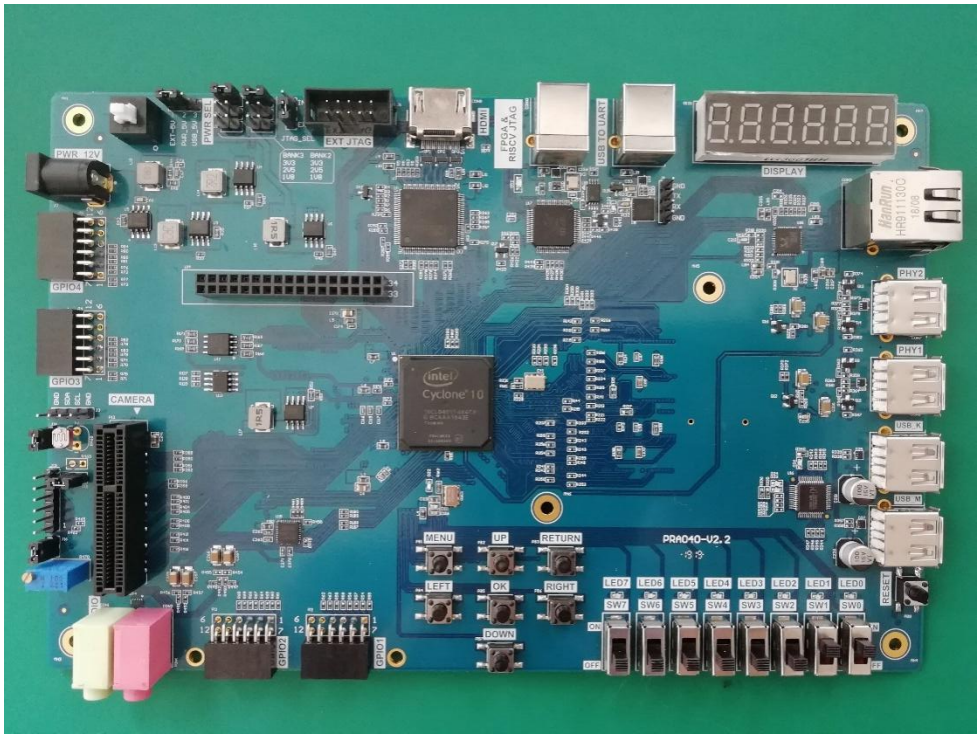
Thank you for purchasing the FPGA development board. Please read the manual carefully before using the product and make sure that you know how to use the product correctly. Improper operation may damage the development board. This manual is constantly updated, and it is recommended that you download the latest version when using.

Official Shopping Website:

https://fpgamarketing.com/FII-PRA040-Altera-risc-v-Cyclone10-FPGA-Boards-FII-PRA040.htm

Contents

Fraser Innovation Inc develops FII-PRA040 based on Intel Cyclone10 series development board. It was initial released in 2018. The model is FII-PRA040. It is resource-rich and high-speed, making it an ideal platform for learning and engineering research. This development board has been spent a lot on system design, PCB design, and function creation. It can be described as "comprehensive and powerful."



PRA040 Board Full View

1. Introduction

This development board uses Intel's Cyclone10 series chip, model 10CL040YF484C8G, which is currently Intel's latest generation FPGA device.

The Cyclone10 series is Intel's latest generation of FPGAs for the data torrent of the future and the rapidly growing IoT application market. This series provides fast, power-saving processing and is suitable for automotive, industrial automation, professional audio and visual systems and a variety of applications. Compared to previous generations of Cyclone FPGAs, the 10 Series saves more power while delivering twice the performance.

PRA040 system block diagram:

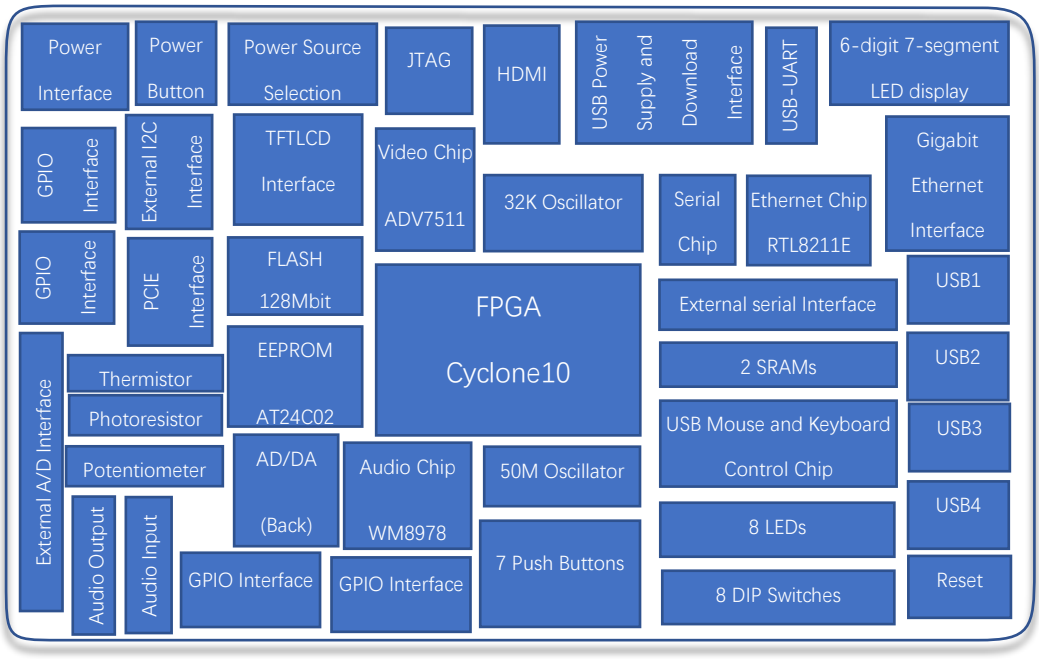


Figure 1.1 PRX100 System Block Diagram

Hardware resources:

- It can be powered by external 12V DC source or by “USB Power Supply and Download Interface”. The latter also provides program download functionality. Only one wire is to complete the power supply and download functions;
- A 50 MHz oscillator, a 32.768 kHz oscillator, provides a stable clock source for the development board;
- 6-digit common anode 7-segment decoders, through dynamic scanning to achieve data display;
- 1 HDMI interface displaying color pictures or camera video;
- 1 EEPROM chip with I2C interface, type AT24C02;
- 1 adaptive 10M/100M/Gigabit Ethernet interface;
- 8 push buttons, 7 for programmable buttons, 1 for reset button;
- 1 photoresistor, through which it can simulate light control; 1 thermistor, which can collect temperature or analog temperature alarm function; 1 potentiometer, which can simulate voltage change;
- 1 PCF8591 AD/DA conversion chip, reserved external interface, free input and output;
- On-board 50MHz and 32.768kHz oscillators provide stable clock signals to the development board;

- 8-bit DIP switch;
- 8-bit LED;
- 1 128Mbit Flash chip;
- 4 GPIO external signal expansion interfaces, also the PMOD standard interface;
- Two JTAG interfaces, one for the FPGA download debug interface and one for the RISC-V CPU JTAG debug interface. Built-in RISC-V CPU software debugger, no external RISC-V JTAG emulator required;
- 1 UART asynchronous serial interface, which can supply power to the development board at the same time;
- 2 SRAMs with a capacity of 16Mbit;
- a pair of audio input and output interfaces;
- 1 PCIE interface for connecting devices that support this interface, such as the BD5640 camera daughter board;
- 4 USB interfaces, 2 for the mouse and keyboard interface, 2 for the universal serial interface;
- 1 USB (USB-B) to UART interface for serial communication;

- 1 TFTLCD touch screen interface, which can realize the display and operation of the touch screen;

Note: Before using development board, you need to check the following

1) Power supply jumper J1. If you are using an external power supply interface, use a jumper cap to connect the two jumpers "EXT_5V" and "PWR_5V". If you are using the "FPGA & RISCV JTAG" interface to supply power, please connect "USB_5V" and "PWR_5V". As shown below:

Figure 1.2 External Power Supply Interface

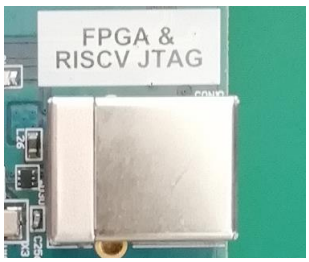


Figure 1.3 USB Power Supply and Download Interface

Figure 1.4 Power Selection Jumper J1

2) Part of the FPGA BANK voltage is determined by selection jumpers. Voltage in development board, in order to adapt to a variety of external signals, is adjustable power supply, specifically by three common voltage

options, 3.3V, 2.5V, and 1.8V. Before the development board works, please make sure that the jumpers of BANK voltage are connected. By default, you will be connected to 3.3V. As shown below:

Figure 1.5 BANK Voltage Selection

3) The program download selection is jumper J7. The development board has two kinds of program download methods, one is to use the external downloader to connect to the JTAG interface to download; the other is to use the provided USB cable to connect to the " FPGA & RISCV JTAG" interface to download. J7 decides which way to use it. J7 “EXT” connection is downloaded using the JTAG interface, and connection “INT” is downloaded using the USB cable. As shown below:

Figure 1.6 Program Download Selection Jumper J7

2. Basic Features

The schematics quoted in this article are intended to highlight the key points, and the circuits that are not related to the theme (such as protection circuits or filter circuits) will be eliminated. Please pay attention to that. For the source material, please refer to the attached schematic.

1) FPGA

As mentioned above, this development board FPGA model is 10CL040YF484C8G, which is Intel's latest generation of low-power high-performance FPGA.

Figure 2.1 FPGA Physical Picture

Chip resources:

Resource		Device
		10CL040
Logic Elements (LE)		39,600
M9K Memory	Block	126
	Capacity (Kb)	1,134
18 x 18 Multiplier		126
PLL		4
Clock		20

Maximum I/O	**325**
Maximum LVDS	**124**

Figure 2.2 Chip Resources

2）Power Supply Interface

The development board has two power supply modes, one is for external 12V DC power supply. (please use the power supply that comes with the development board, do not use other specifications of the power supply to avoid damage to the development board) Its power supply interface is as follows:

Figure 2.3 External Power Supply Interface

The second way is to use the USB cable to connect the “FPGA & RISCV JTAG" interface. See Figure 2.4.

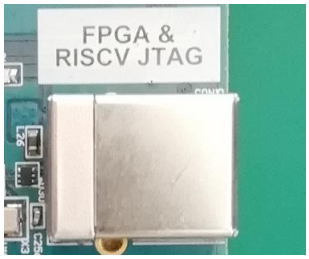


Figure 2.4 Internal Power Supply Interface

It should be noted that regardless of the power supply method, the power selection jumper needs to be connected to the correct position. As shown below:

Figure 2.5 Power Supply Selection Jumpers

By the way to mention the power supply circuit of the development board and the power supply of the FPGA. The external 12V power supply is converted to a 5V power supply through the U5 power supply chip and connected to the pin 1 of J1. The "PC_USB5V" power supply from the USB port is connected to the pin 3 of J1. With which of the two is connected to the 2nd pin, it powers the development board. There is no problem when the two power supplies are connected at the same time.

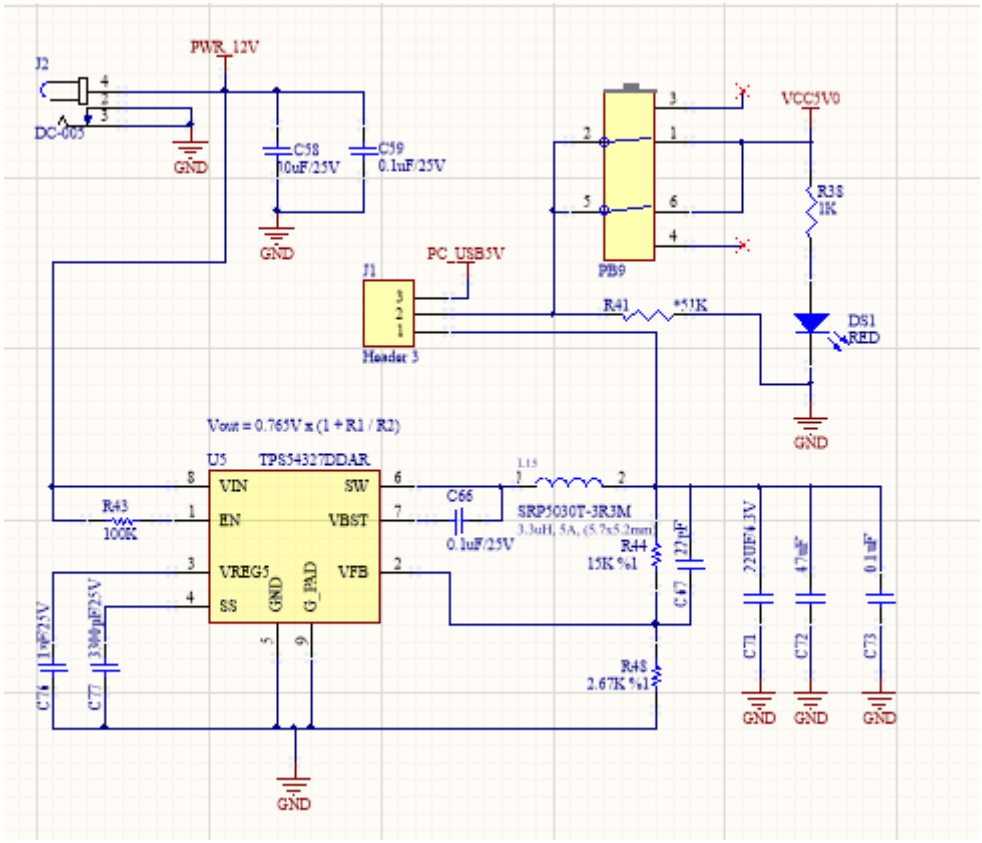


Figure 2.6 External Power Supply Schematics

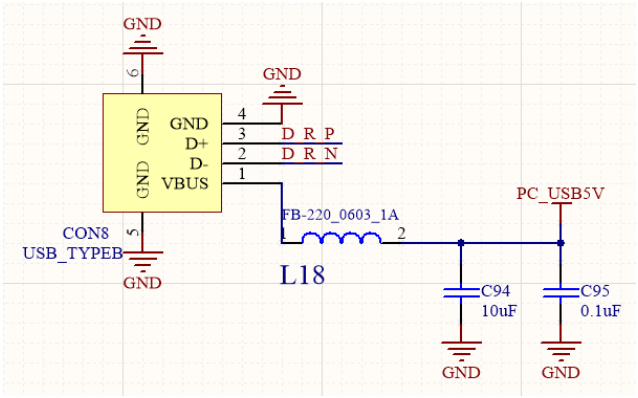


Figure 2.7 USB Power Supply Interface Schematics

We can see that after the PB9 is turned on, the power supply is connected to the VCC5V0 level network of the development board, and then converted to the 1.2V (FPGA core voltage), 1.8V, 2.5V, or 3.3V. Among them, 1.8V, 2.5V, and 3.3V are

the BANK voltage of the FPGA. The three voltages are provided to meet the level standards of various external signals. The conversion circuit is shown below.

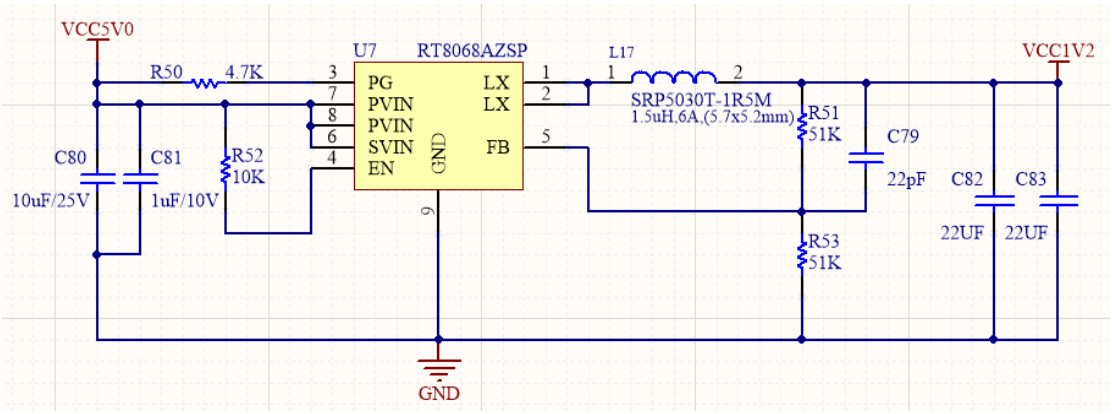


Figure 2.8 Schematics of the 1.2V Power Supply

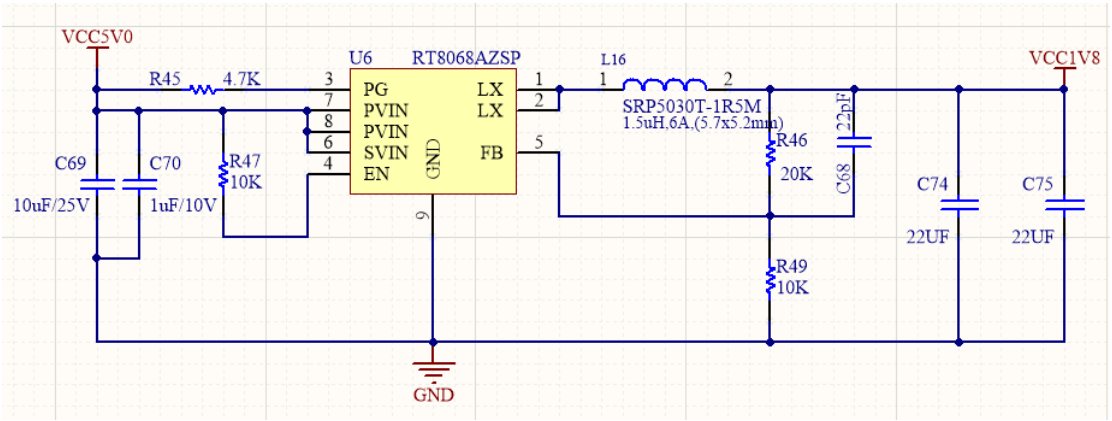


Figure 2.9 Schematics of the 1.8V Power Supply

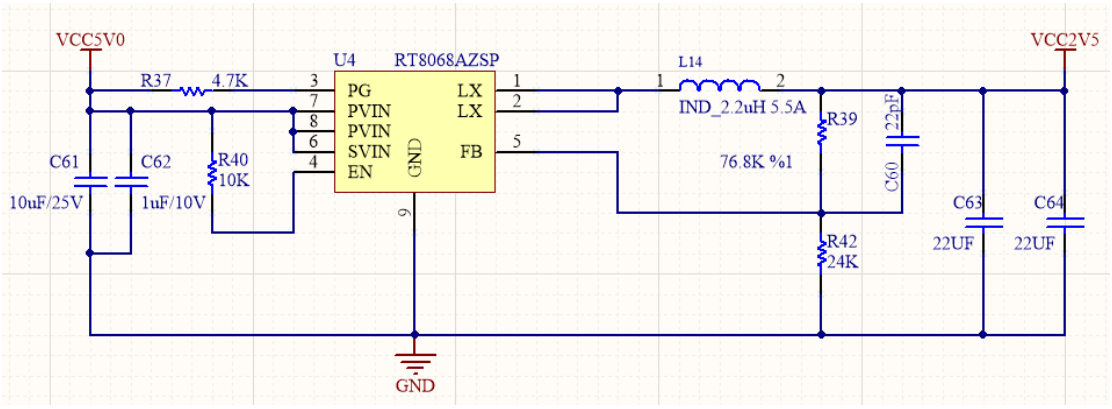


Figure 2.10 Schematics of the 2.5V Power Supply

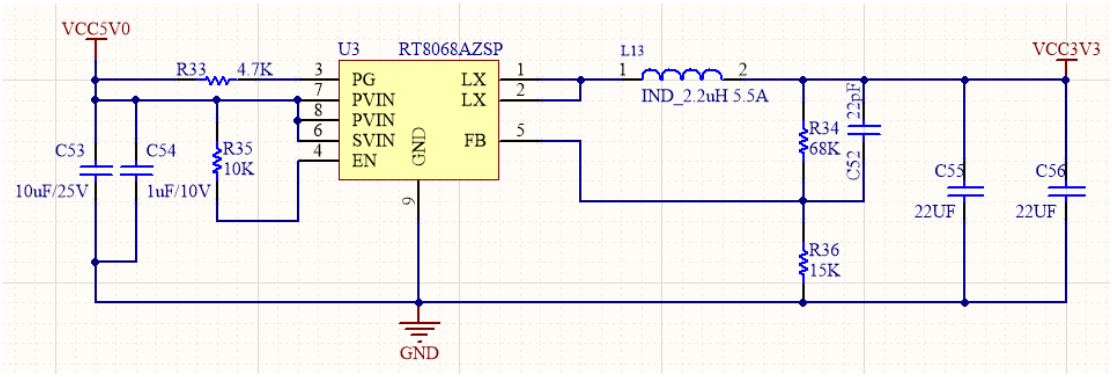


Figure 2.11 Schematics of the 3.3V Power Supply

If we look at the power supply of the FPGA, we can see these kinds of voltages (to highlight the topic, the screenshot skips the irrelevant circuit):

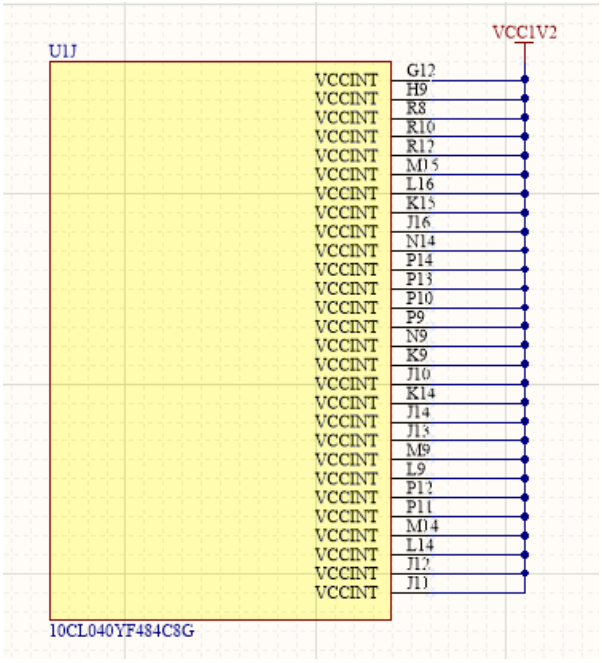


Figure 2.12 Schematics of the FPGA Power Supply 1

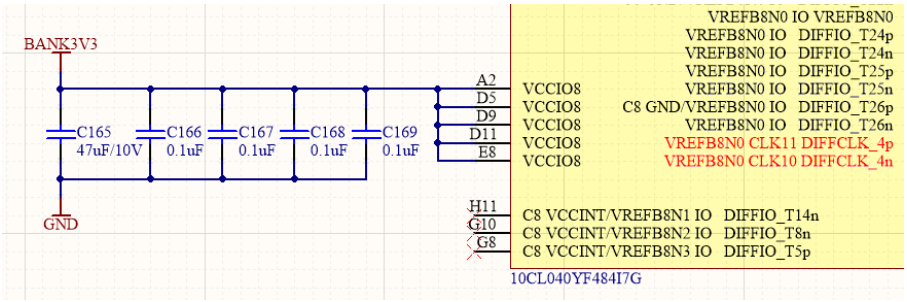


Figure 2.13 Schematics of the FPGA Power Supply 2

In Figure 2.12 and Figure 2.13, VCCINT is the core power pin of the FPGA, and the pins such as VCCIO8 are the BANK power pins of the FPGA. The G12, H9, R8, etc. next to the wiring are the pin numbers of the FPGA. Some FPGAs are in non-BGA (Ball Grid Array) packages, such as 144-pin, 208-pin FPGA chips. Their pin definitions are pure numbers, such as 1 to 144, 1 to 208, etc. However, for the BGA packaged FPGA chip, the pin names become in the form of letters + numbers, such as E3, G3, etc. In the schematic, BGA package FPGA chip is used. (The other

power supply parts of the FPGA are not listed. For details, please refer to the schematics).

3) Oscillator

Two on-board oscillators, one for 50MHz and the other for 32.768KHz. The clock inputs are connected to the G21 and AA12 pins of the FPGA. The schematic is as follows:

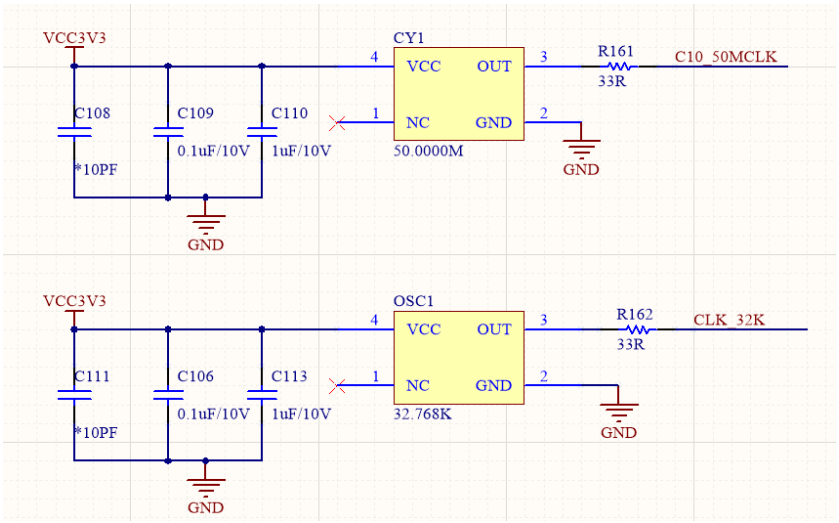


Figure 3.1 Schematics of Oscillators

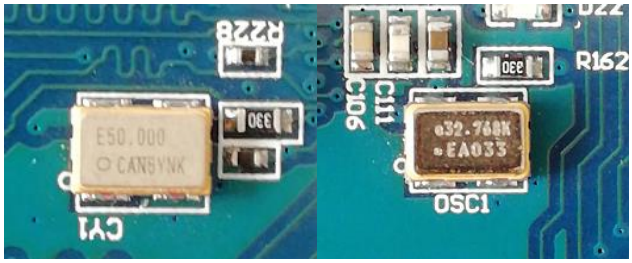


Figure 3.2 Oscillators Physical Picture

Pin Assignment

Signal Name	FPGA Pin

CLK_32.768K	AA12
CLK_50M	G21

4) Segment LED Display

Figure 4.1 Segment Display Decoders

One type of segment display is a semiconductor light-emitting device. The segment display can be divided into a seven-segment display decoder and an eight-segment display decoder. The difference is that the eight-segment display decoder has one more unit for displaying the decimal point, the basic unit is a light-emitting diode. The segment structure of the decoder is shown below:

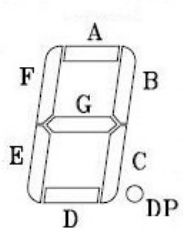


Figure 4.2 Segment Display Decoder Structure

Common anode decoders are used here. That is, the anodes of the LEDs are connected.

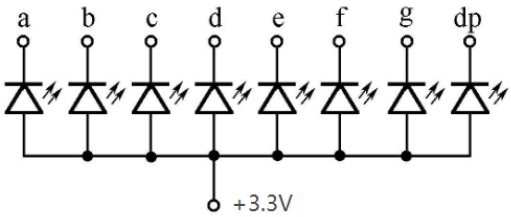


Figure 4.3 Schematics of Common Anode Decoders

To illuminate a segment of an 8-segment display decoder, the level of the corresponding pin needs to be pulled low; when the pin is set high, the corresponding field will not light. This development board uses a 6-in-one eight-segment decoder. The schematics is shown below:

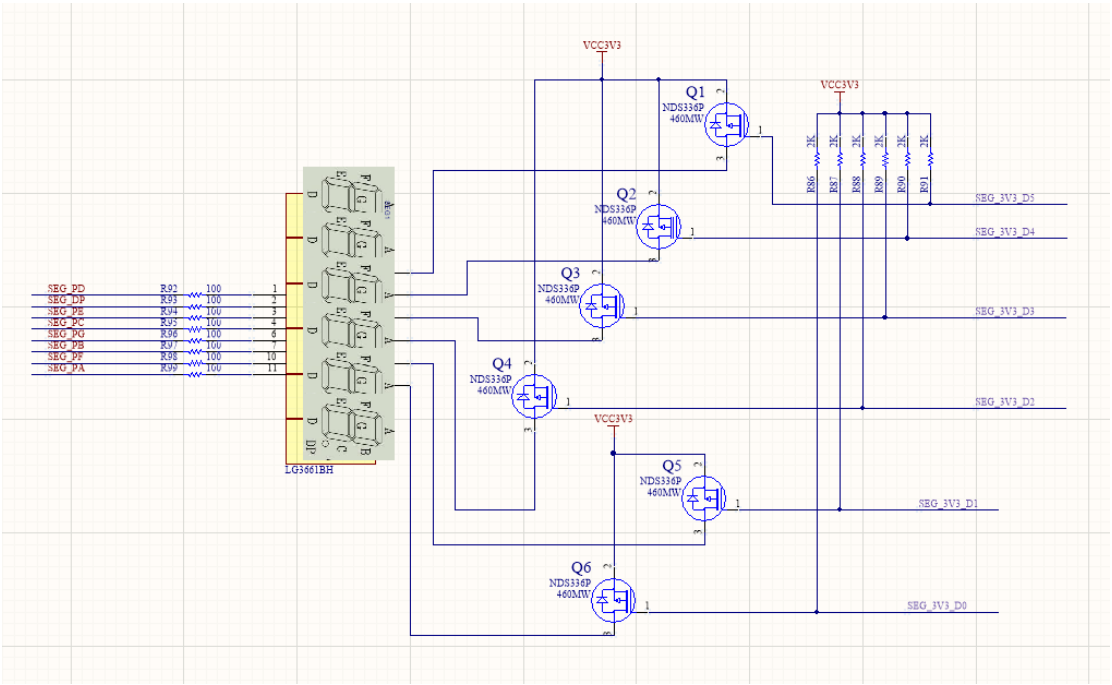


Figure 4.4 Schematic of Display Decoders

The six-in-one display decoder is a dynamic display. Due to the persistence of human vision and the afterglow effect of the LED, although the decoders are not lit at the same time, if the scanning speed is fast enough, the impression of human

eyes is a group of stable display data, no flickering can be noticed. The same segments of the six-in-one decoders are connected, a total of eight pins, and with six control signal pins, a total of 14 pins, as shown in Figure 4.4. Among them SEG_PA, SEG_PB, SEG_PC, SEG_PD, SEG_PE, SEG_PF, SEG_PG, SEG_DP correspond to the A, B, C, D, E, F, G, DP of decoder; SEG_3V3_D [0..5] are six control pins of the decoders, which are also active low. When the control pin is low, the corresponding decoder is powered, so that the LED can be lit.

Pin assignments of display decoders

Signal Name	FPGA Pin	Description
SEG PA	B15	Segment A
SEG PB	E14	Segment B
SEG PC	D15	Segment C
SEG PD	C15	Segment D
SEG PE	F13	Segment E
SEG PF	E11	Segment F
SEG PG	B16	Segment G
SEG DP	A16	Segment DP
SEG_3V3_D0	F14	Decoder 1(from right)
SEG_3V3_D1	D19	Decoder 2(from right)
SEG_3V3_D2	E15	Decoder 3(from right)
SEG_3V3_D3	E13	Decoder 4(from right)
SEG_3V3_D4	F11	Decoder 5(from right)
SEG_3V3_D5	E12	Decoder 6(from right)

5）HDMI Interface

Image display processing has always been the focus of FPGA research. At present, the image display mode is also constantly developing. The image display interface is also gradually transitioning from the old VGA interface to the new DVI or HDMI interface. HDMI is the abbreviation of High Definition Multimedia Interface. It is a digital video/audio interface technology, which is a dedicated digital interface for image transmission. It can transmit audio and video signals at the same time.

The ADV7511 is a chip that converts FPGA digital signal to HDMI signal following VESA standard. For details, see the related chip manual. Among them, ADV7511_Programming_Guide and ADV7511_Hardware_Users_Guide are the most important. You can configure the registers of ADV7511 by viewing this document.

Figure 5.1 HDMI Interface and ADV7511 Chip

HDMI pin assignment

Signal Name	FPGA Pin
HDMI- INT	D10
HDMI- SCL	D13

HDMI-SDA	C13
HDMI-VSYNC	A9
HDMI-HSYNC	B9
HDMI-CLK	E5
HDMI-HPD	E6
HDMI-D35	G7
HDMI-D34	F9
HDMI-D33	F7
HDMI-D32	C3
HDMI-D31	B3
HDMI-D30	C4
HDMI-D29	A3
HDMI-D28	E7
HDMI-D23	B4
HDMI-D22	D6
HDMI-D21	A4
HDMI-D20	C6
HDMI-D19	B5
HDMI-D18	D7
HDMI-D17	C7
HDMI-D16	A5
HDMI-D11	B6
HDMI-D10	F8
HDMI-D9	A6
HDMI-D8	C8

HDMI-D7	B7
HDMI-D6	E9
HDMI-D5	B8
HDMI-D4	A7
HDMI-DE	A8
HDMI-SPDIF	C10
HDMI-I2S0	B1
HDMI-I2S1	E1
HDMI-I2S2	E4
HDMI-I2S3	E3
HDMI-SCLK	B10
HDMI-LRCLK	A10

6）EEPROM

EEPROM is generally used in the instrumentation design. It is often used as a storage for some parameters. Data is not lost when power is off, and it is easy to operate. It is an ideal storage device.

The development board contains an EEPROM, model AT24C02, with a capacity of 2kbit (256*8bit), consisting of a 256-byte block that communicates over the IIC bus.

IIC (Inter-Integrated Circuit) literally means between integrated circuits, which is the IIC Bus abbreviation. It is a serial communication bus, using multi-master-

slave architecture, by Philips in the 1980s, developed to allow motherboards, embedded systems, or mobile phones to connect to low-speed peripherals. Also written as "I²C", "I2C", the correct reading is "I-squared-C".

The onboard EEPROM is designed to learn how the IIC bus communicates. See Figure 6.1 for the schematics.

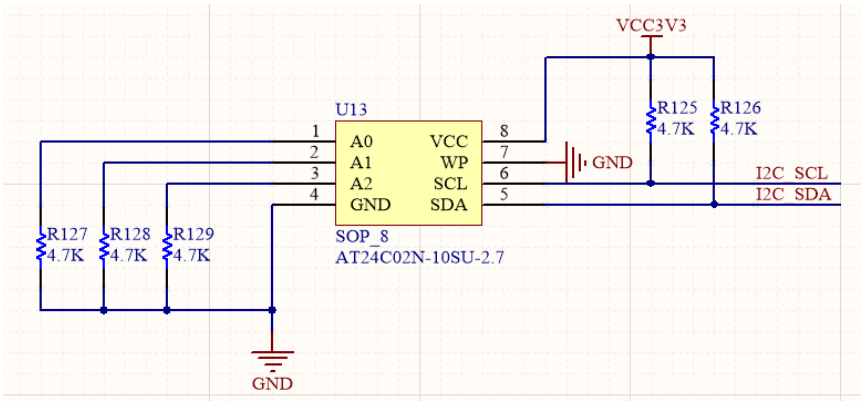


Figure 6.1 Schematics of EEPROM

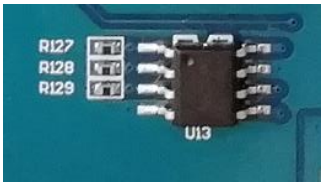


Figure 6.2 Physical Picture of EEPROM

EEPROM pin assignment

Signal Name	FPGA Pin
SCL	D13
SDA	C13

7）Gigabit Ethernet Interface

Ethernet is currently the most commonly used data communication method. Ethernet is getting faster and faster from the initial 10Mb/s to the later 100Mb/s，and to 1000Mb/s now.

The development board is equipped with an RTL8211E Gigabit Ethernet chip. The RTL8211E is a highly integrated network receiving PHY chip from Realtek. It is compliant with 10Base-T, 100Base-TX and 1000Base-T IEEE802.3 standards. It can transmit network data via CAT 5 UTP cable and CAT 3 UTP cable. It belongs to the physical layer in network communication and is used for data communication between MAC and PHY. Mainly used in network interface adapters, network hubs, gateways and some embedded devices.

The main features of the RTL8211E include:

- Meets 1000Base-T IEEE802.3ab standard
- Compliant with 100Base-TX IEEE802.3u standard
- Compliant with 10Base-T IEEE802.3 standard
- Support IEEE 802.3 RGMII interface
- Support IEEE 802.3 GMII, MII interface, only RTL8211EG support
- Support for Wake-on-LAN
- Support for interrupt function

- Support crossover detection and auto-correction
- Support half-duplex, full-duplex operation
- 1000 MHz communication CAT 5 network cable can reach 100m
- RGMII interface supports 3.3V, 2.5V, 1.8V, 1.5V signals
- LED indications for three network states are available

See below for the schematics.

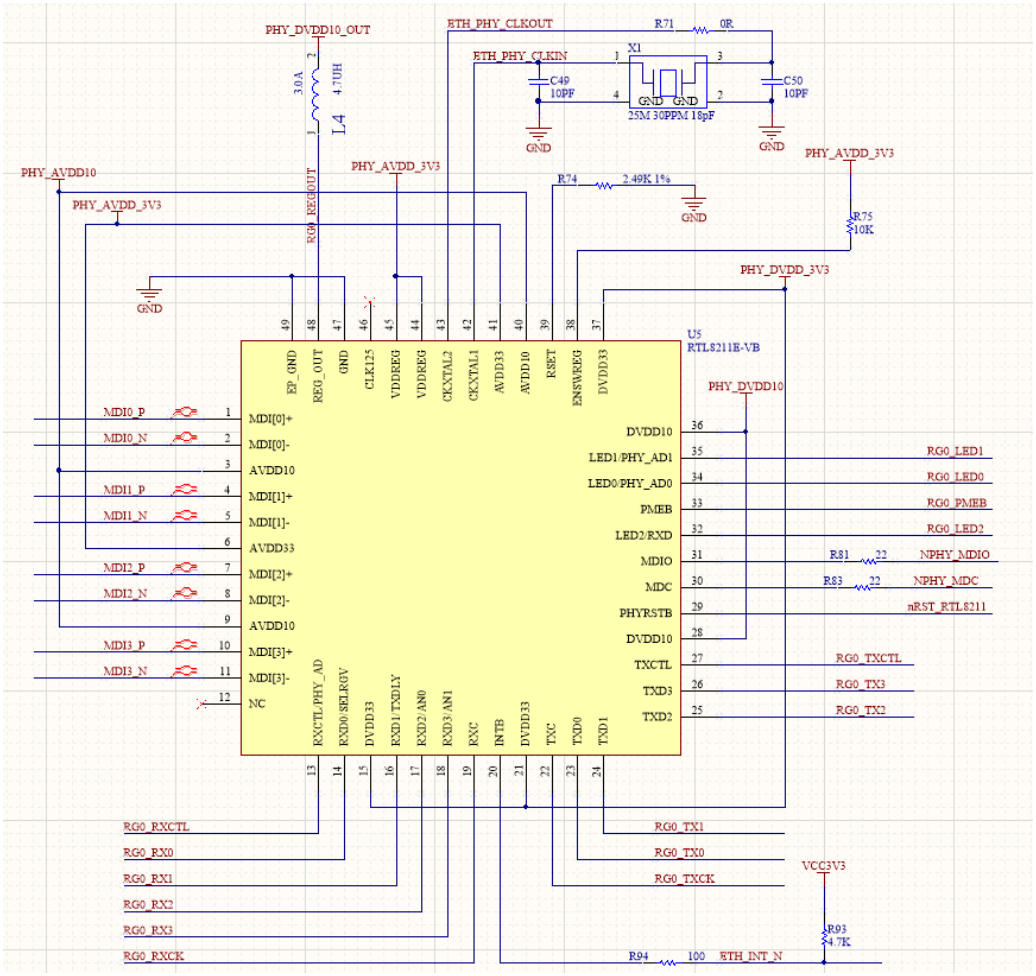


Figure 7.1 Schematics of Gigabit Ethernet Chip

Figure 7.2 Gigabit Ethernet Physical Picture

Gigabit ethernet pin assignment

Signal Name	FPGA Pin
RG0_RXCTL	A13
RG0_RXD0	B13
RG0_RXD1	A14
RG0_RXD2	B14
RG0_RXD3	A15
RG0_RXCK	B12
RG0_TXCK	B20
RG0_TXD0	A17
RG0_TXD1	B17
RG0_TXD2	A18
RG0_TXD3	B18
RG0_TXCTL	A13
NPHY_MDC	C17
NPNY_MDIO	B19
ETH_INT_N	D17
PHYRSTB	C19

8）Push Button

The development board has 8 push buttons, 7 of which are programmable buttons and 1 is for system reset. The default is set high and can be pressed low. Schematics is shown in Figure 8.1.

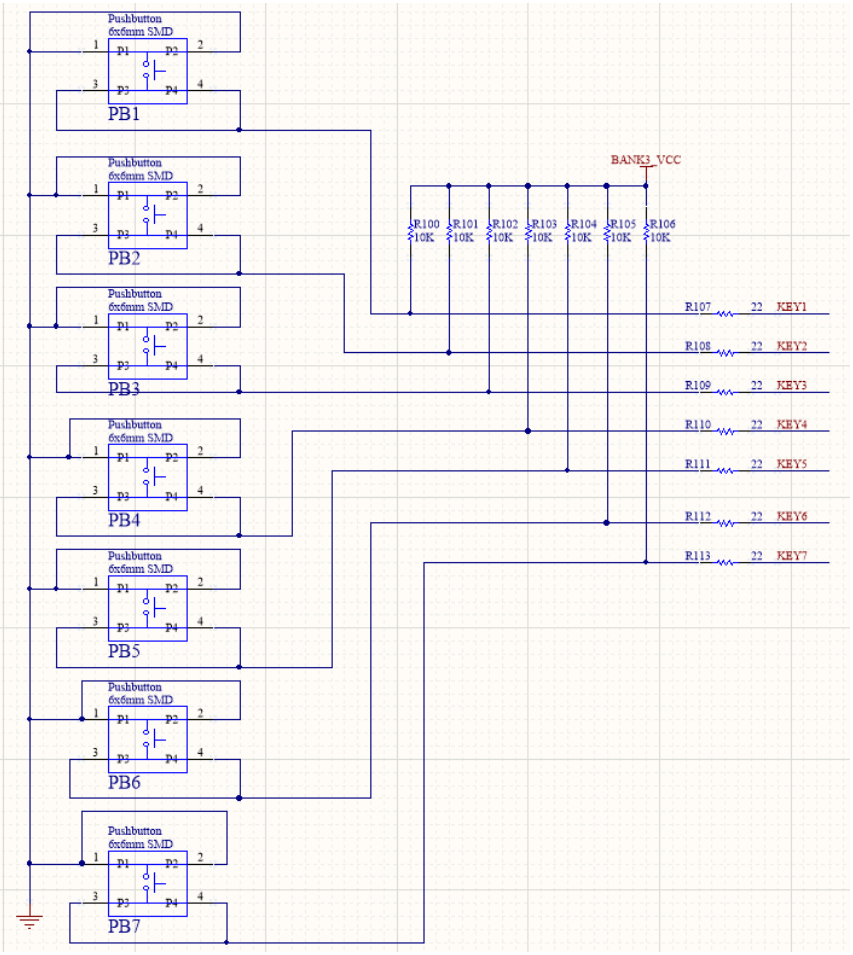


Figure 8.1 Schematics of Push Buttons

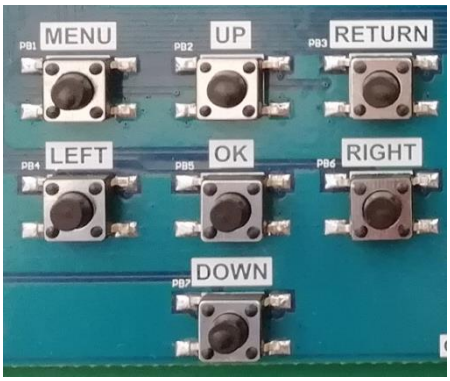


Figure 8.2 Push Button Physical Picture

Push button pin assignment

Signal Name	FPGA Pin
PB1(MENU)	Y4
PB2(UP)	V5
PB3(RETURN)	Y6
PB4(LEFT)	AB4
PB5(OK)	Y3
PB6(RIGHT)	AA4
PB7(DOWN)	AB3

9) AD/DA Thermistor, Photoresistor and Potentiometer

The PCF8591 chip is a monolithically integrated, individually powered, low power consuming, 8-bit CMOS data acquisition device. It has 4 analog inputs, 1 analog output, and 1 serial I2C bus interface. The three address pins A0, A1 and

A2 of PCF8591 can be used for hardware address programming (the three addresses on the development board are connected to GND, that is, the device address is 7'B1001000), allowing access on the same I2C bus. PCF8591 devices without additional hardware. The address, control, and data signals input and output on the PCF8591 device are serially transmitted over a two-wire bidirectional I2C bus. Chip features of PCF8591:

- Operating voltage range 2.5V-6V
- Low standby current
- Serial input/output via I2C bus
- I2C address selection by 3 hardware address pins
- Max sampling rate given by I2C bus speed
- 4 analog inputs configurable as single ended or differential inputs
- Auto-incremented channel selection
- Analog voltage ranges from VSS to VDD
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output

The schematics is shown in Figure 9.1 (to make the theme clearer, the figure has been modified for the design drawings):

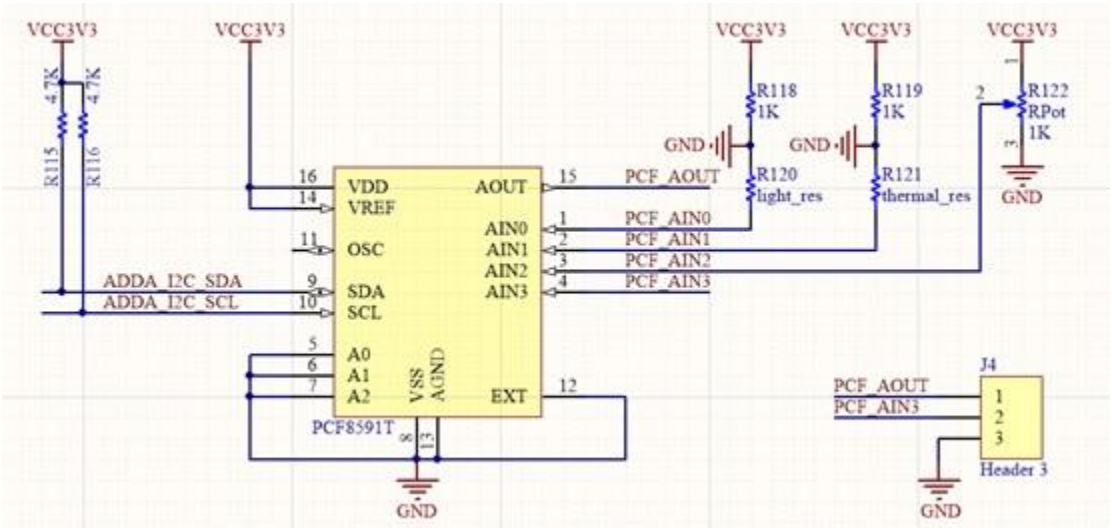


Figure 9.1 Schematics of AD/DA

Figure 9.2 PCF8591 Physical Picture

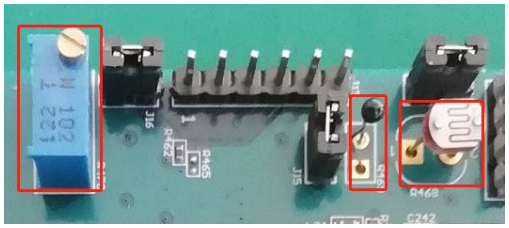


Figure 8.3 Potentiometer, Photoresistor, and Thermistor

When using a potentiometer, connect J16 with a jumper cap. When using the thermistor, connect J15. When using a photoresistor, connect J14.

PCF8591 pin assignment

Signal Name	FPGA Pin
ADDA_I2C_SAD	D20
ADDA_I2C_SCL	C20

10）DIP Switch

The 8-bit DIP switch is onboard, and the FPGA pin gets high when the switch is turned on. The schematics is shown as follows:

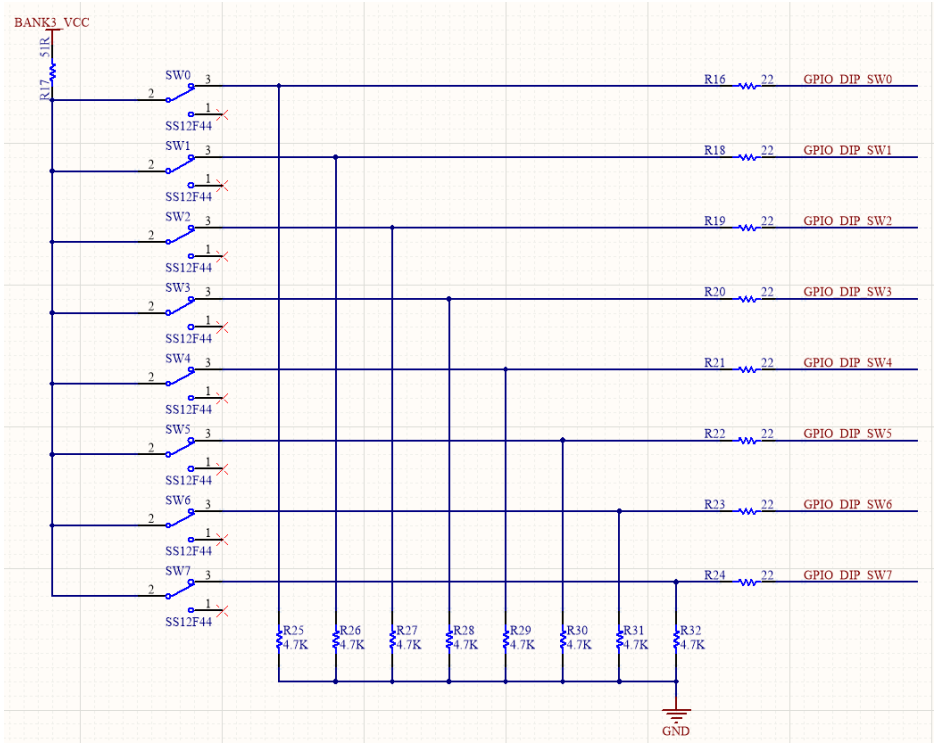


Figure 10.1 Schematics of DIP Switches

Figure 10.2 DIP Switches Physical Picture

DIP switches pin assignment

Signal Name	FPGA Pin
SW0	U11
SW1	V11
SW2	U10
SW3	V10
SW4	V9
SW5	W8
SW6	Y8
SW7	W6

11）LED

The development board has eight LEDs. When the pin is low, the LED emits light, and when it is high, the LED does not emit light. The schematic is shown in Figure 11.1.

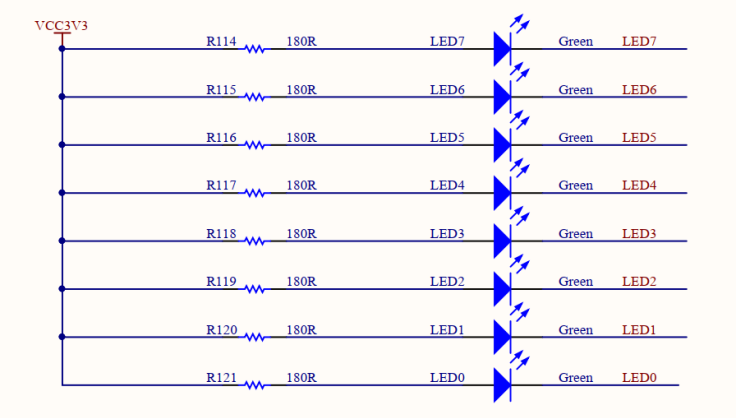


Figure 11.1 Schematics of LED

Figure 11.2 LED Physical Picture

LED pin assignment

Signal Name	FPGA Pin
LED0	J5
LED1	J6
LED2	H5
LED3	H6
LED4	H7
LED5	G5
LED6	F1
LED7	F2

12）FLASH

The N25Q128A is a serial FLASH chip with a capacity of 128Mbit, which is more than enough for storing programs in the FPGA. Figure 12.1 shows the N25Q128A in the schematics.

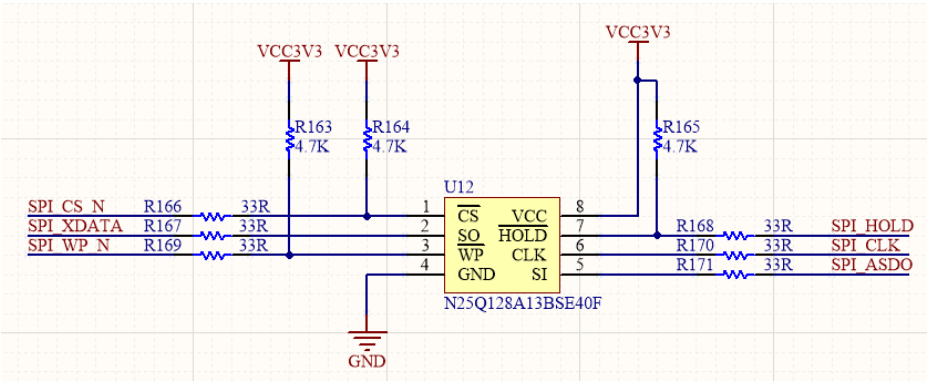


Figure 12.1 Schematics of FLASH

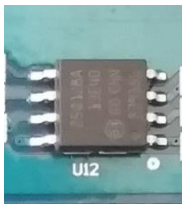


Figure 12.2 FLASH Physical Picture

13）GPIO（PMOD）Expansion Interface

The development board has four GPIO interfaces and is also a standard PMOD interface. The P1 and P2 interfaces each contain 6 standard IO pins of PFGA resources, 2 GND signals, and 2 adjustable power signals. The P3 and P4 interfaces contain 4 pairs of LVDS signals, which can also be used as 8 standard IOs; 2 GND signals, and 2 adjustable power signals. It can be used with the BD5640-PMOD camera daughter board or the BD9226 high-speed AD daughter

board. The daughter boards are available at the official online store. The schematics is as follows:

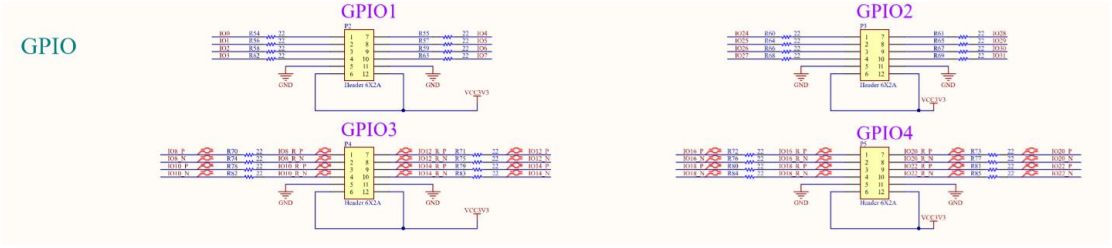


Figure 13.1 Schematics of GPIO

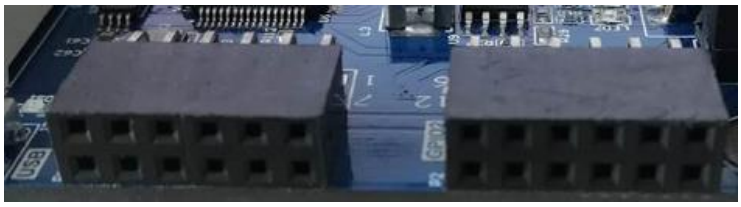


Figure 13.2 GPIO Physical Picture

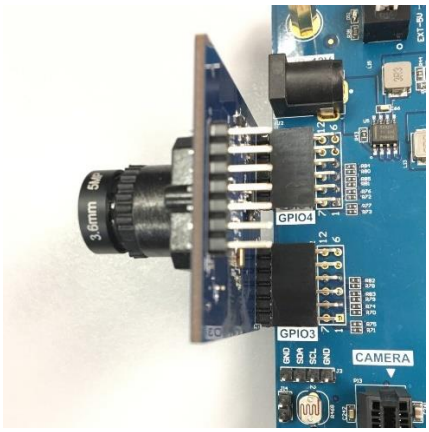


Figure 13.3 GPIO Interface with BD5640-PMOD Camera Daughter Board

Figure 13.4 GPIO Interface with BD9226 High-speed AD Daughter Board

GPIO pin assignment

Signal Name	FPGA Pin	Description
GPIO1-Pin 1	AA20	Standard IO
GPIO1-Pin 2	R16	Standard IO
GPIO1-Pin 3	V16	Standard IO
GPIO1-Pin 4	AA15	Standard IO
GPIO1-Pin 5		GND
GPIO1-Pin 6		VCC3V3
GPIO1-Pin 7	AB20	Standard IO
GPIO1-Pin 8	U17	Standard IO
GPIO1-Pin 9	T16	Standard IO
GPIO1-Pin 10	U16	Standard IO
GPIO1-Pin 11		GND
GPIO1-Pin 12		VCC3V3
GPIO2-Pin 1	AA14	Standard IO
GPIO2-Pin 2	W13	Standard IO
GPIO2-Pin 3	AB13	Standard IO
GPIO2-Pin 4	V12	Standard IO
GPIO2-Pin 5		GND
GPIO2-Pin 6		VCC3V3
GPIO2-Pin 7	R14	Standard IO
GPIO2-Pin 8	AB14	Standard IO
GPIO2-Pin 9	Y13	Standard IO
GPIO2-Pin 10	AA13	Standard IO
GPIO2-Pin 11		GND

GPIO2-Pin 12		VCC3V3
GPIO3-Pin 1	U9	LVDS1-P
GPIO3-Pin 2	V8	LVDS1-N
GPIO3-Pin 3	W7	LVDS2-P
GPIO3-Pin 4	Y7	LVDS2-N
GPIO3-Pin 5		GND
GPIO3-Pin 6		VCC3V3
GPIO3-Pin 7	W10	LVDS3-P
GPIO3-Pin 8	Y10	LVDS3-N
GPIO3-Pin 9	AA10	LVDS4-P
GPIO3-Pin 10	AB10	LVDS4-N
GPIO3-Pin 11		GND
GPIO3-Pin 12		VCC3V3
GPIO4-Pin 1	AA8	LVDS5-P
GPIO4-Pin 2	AB8	LVDS5-N
GPIO4-Pin 3	AA7	LVDS6-P
GPIO4-Pin 4	AB7	LVDS6-N
GPIO4-Pin 5		GND
GPIO4-Pin 6		VCC3V3
GPIO4-Pin 7	AA9	LVDS7-P
GPIO4-Pin 8	AB9	LVDS7-N
GPIO4-Pin 9	AA5	LVDS8-P
GPIO4-Pin 10	AB5	LVDS8-N
GPIO4-Pin 11		GND
GPIO4-Pin 12		VCC3V3

14）JTAG Interface

The development board provides two JTAG interfaces, two programming download modes, which are selected by an SN74CBTLV3257 multiplexer when downloading the FPGA program. The selection pin of the SN74CBTLV3257 is connected to the J7 jumper. The JTAG schematics is shown in Figure 14.1:

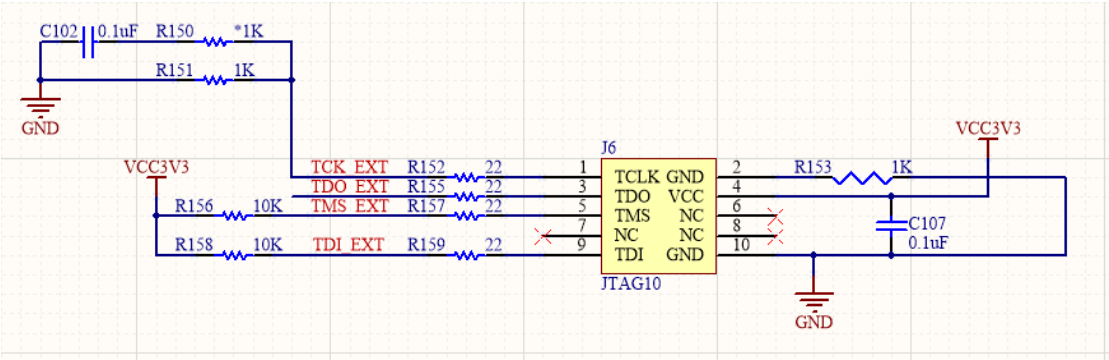


Figure 14.1 Schematics of JTAG Interface 1

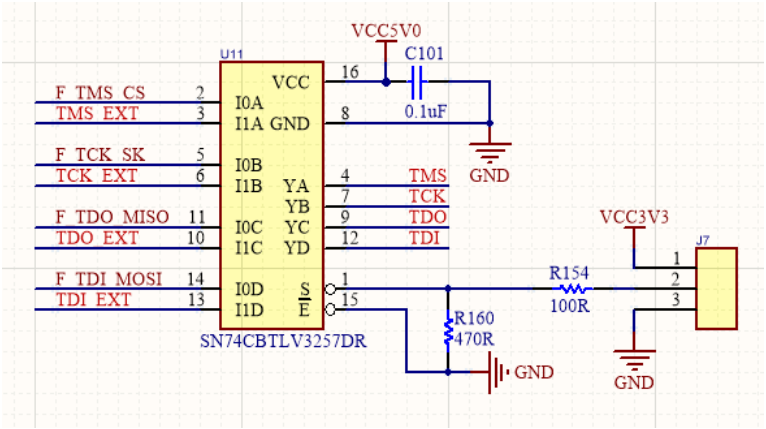


Figure 14.2 Schematics of JTAG Interface 2

Figure 14.3 JTAG Interface Physical Picture

JTAG pin assignment

Signal Name	FPGA Pin
TCK-1Pin	L2(TCK)
TDO-3Pin	L4(TDO)
TMS-5Pin	L1(TMS)
TDI-9Pin	L5(TDI)

The second JTAG interface is “FPGA & RISCV JTAG”, which downloads the program for the RISC-V CPU. The physical picture and pin assignments are as follows:

Figure 14.3 RISC-V Download Interface Physical Picture

RISC-V download interface pin assignment

Signal Name	FPGA Pin
CPU_TTDO	H2

CPU_TSRST_n	J3
CPU_TRST_n	J2
CPU_TRTCK	J4
CPU_TTDI	H1
CPU_TTMS	J1
CPU_TTCK	G2

15）UART Interface

A USB-B interface and a CP2102 chip are onboard for serial data communication.

The CP2102 features a high level of integration with a USB 2.0 full-speed function controller, USB transceiver, oscillator, EEPROM, and asynchronous serial data bus (UART) to support modem full-featured signals without the need for any external USB devices. Its characteristics are as follows

- Integrated USB transceiver; no external resistors required
- Integrated clock; no external oscillator required
- On-chip power-on reset circuit
- On-chip voltage regulator can output 3.3V voltage
- USB Specification 2.0 compliant
- USB suspend states supported via SUSPEND pins

- Asynchronous serial data bus is compatible with all handshake and modulation regulator interface signals
- Supported data formats are data bit 8, stop bit 1, 2 and check digit
- Intrinsic more than 512-byte receive buffer and 512-byte transmit buffer
- Hardware or X-On/X-Off handshaking supported

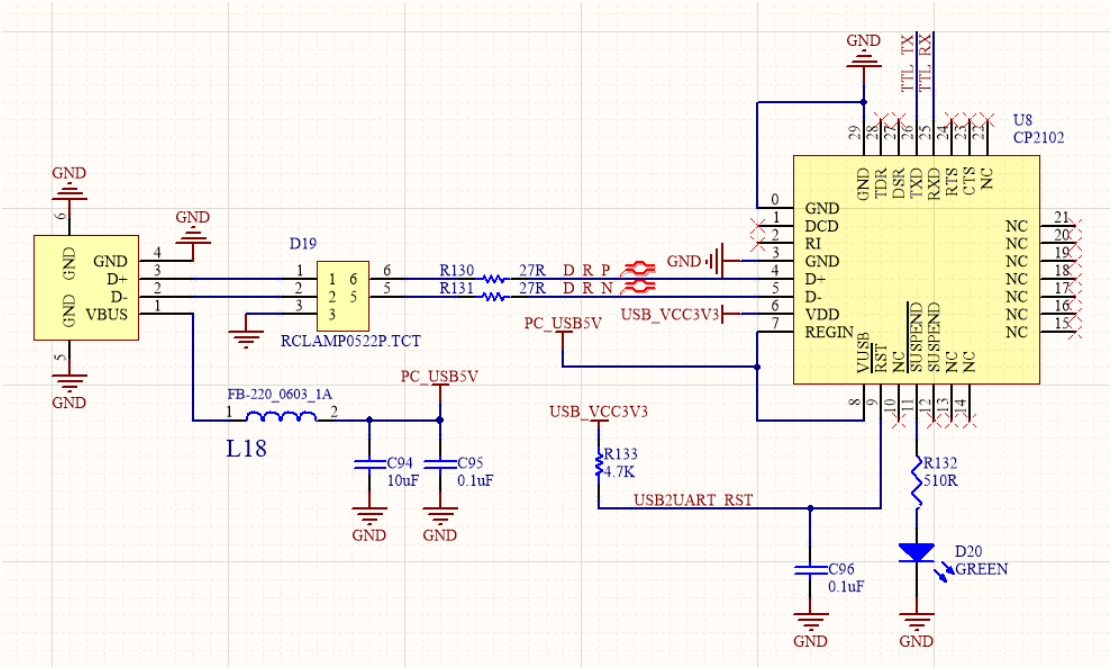


Figure 15.1 UART Schematics

Figure 15.2 USB-B Interface and CP2102 Chip Physical Picture

UART pin assignment

Signal Name	FPGA Pin
TTL_TX/FPGA_RX	F15
TTL_RX/FPGA_TX	E16

16）SRAM

SRAM (Static Random-Access Memory) is a type of random-access memory. The "static" means that if the memory is kept energized, the data stored therein can be kept constant. In contrast, data stored in dynamic random-access memory (DRAM) needs to be updated periodically. However, when the power supply is stopped, the data stored in the SRAM will disappear (called volatile memory), which is different from the ROM or flash memory that can store data after the power is turned off. The development board has two Super SRAMs, which are connected in parallel to a 32-bit data interface. The maximum access space is up to 2M bytes, IS61WV51216 (2 pieces) 512K x 32bit. The design schematics is as follows:

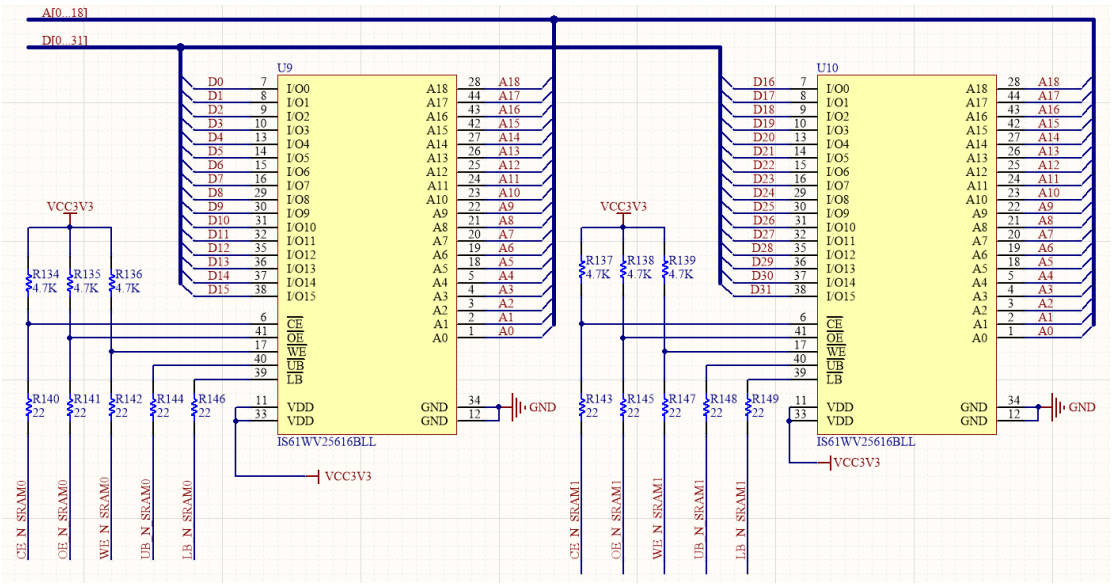


Figure 16.1 Schematics of SRAM

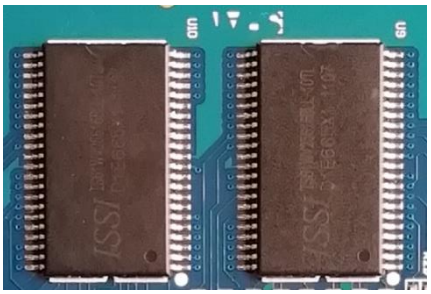


Figure 16.2 SRAM Physical Picture

SRAM pin assignment:

Signal Name	FPGA Pin
SRAM0_CE_N	F21
SRAM0_OE_N	F17
SRAM0_WE_N	B22
SRAM0_UB_N	K22
SRAM0_LB_N	K21
SRAM0_IO0	F22
SRAM0_IO1	E21

SRAM0_IO2	D21
SRAM0_IO3	E22
SRAM0_IO4	D22
SRAM0_IO5	C21
SRAM0_IO6	B21
SRAM0_IO7	C22
SRAM0_IO8	M16
SRAM0_IO9	K19
SRAM0_IO10	M20
SRAM0_IO11	M19
SRAM0_IO12	L22
SRAM0_IO13	L21
SRAM0_IO14	J22
SRAM0_IO15	J18
SRAM0_A0/SRAM1_A0	J21
SRAM0_A1/SRAM1_A1	H22
SRAM0_A2/SRAM1_A2	H19
SRAM0_A3/SRAM1_A3	G18
SRAM0_A4/SRAM1_A4	H17
SRAM0_A5/SRAM1_A5	H21
SRAM0_A6/SRAM1_A6	H20
SRAM0_A7/SRAM1_A7	F19
SRAM0_A8/SRAM1_A8	H18
SRAM0_A9/SRAM1_A9	F20
SRAM0_A10/SRAM1_A10	W21

SRAM0_A11/SRAM1_A11	W22
SRAM0_A12/SRAM1_A12	V21
SRAM0_A13/SRAM1_A13	U20
SRAM0_A14/SRAM1_A14	V22
SRAM0_A15/SRAM1_A15	R21
SRAM0_A16/SRAM1_A16	U21
SRAM0_A17/SRAM1_A17	R22
SRAM0_A18/SRAM1_A18	U22
CE_N_SRAM1	N22
OE_N_SRAM1	Y21
WE_N_SRAM1	R19
UB_N_SRAM1	Y22
LB_N_SRAM1	T18
SRAM1_IO0	M21
SRAM1_IO1	K18
SRAM1_IO2	N21
SRAM1_IO3	M22
SRAM1_IO4	P22
SRAM1_IO5	P20
SRAM1_IO6	R20
SRAM1_IO7	P21
SRAM1_IO8	W19
SRAM1_IO9	W20
SRAM1_IO10	R17
SRAM1_IO11	T17

SRAM1_IO12	U19
SRAM1_IO13	AA21
SRAM1_IO14	AA22
SRAM1_IO15	R18

17）Audio

There is a piece WM8978 onboard, which is a stereo multimedia digital signal codec with speaker driver. The WM8978 is a low power, high quality stereo multimedia digital signal codec. It is mainly used in portable applications such as digital cameras and portable digital camcorders. It combines stereo differential microphone preamplifiers with speakers, headphones and differential, stereo line output drivers to reduce the external components necessary for the application, such as advanced on-chip digital signal processing function with separate microphone or headphone amplifiers, including a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. The WM8978 digital audio interface can operate as a master or a slave. An internal PLL can generate all required audio clocks for the CODEC from common reference clock frequencies.

The design schematic is as follows

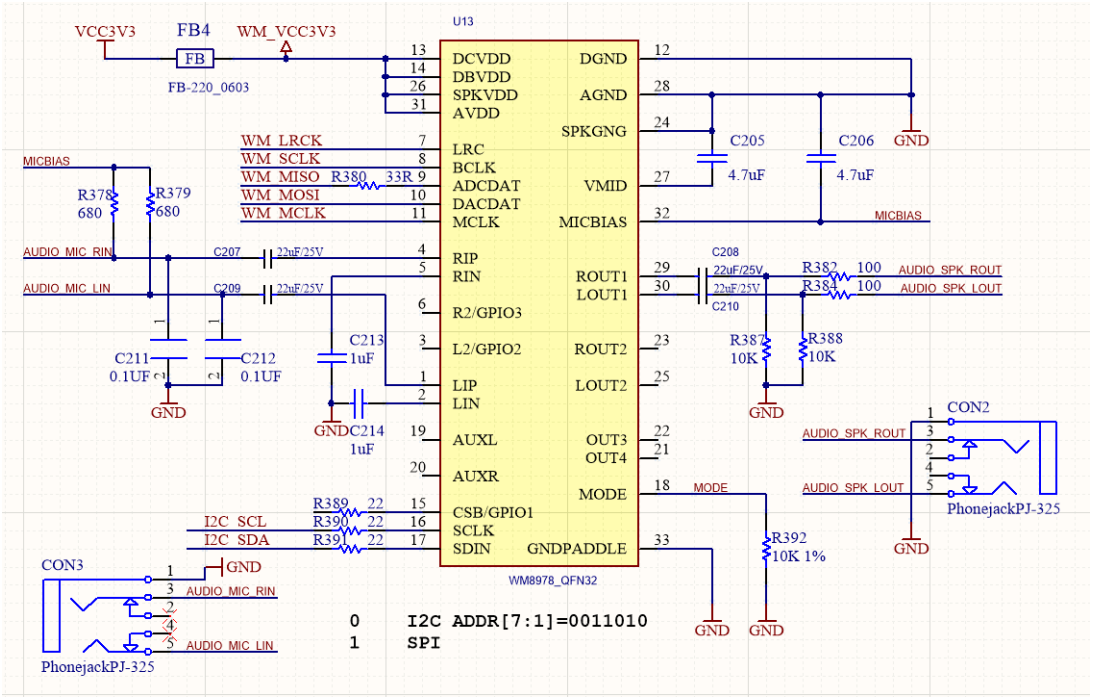


Figure 17.1 Schematics of Audio

Figure 17.2 Audio Interface and Chip Physical Picture

Pin assignment

Signal Name	FPGA Pin
WM_LRC	AB19
WM_BCLK	AA19
WM_ADCDAT	Y17
WM_DACDAT	AA18
WM_MCLK	W17
WM_SCLK	D13
WM_SDIN	C13

18）USB Keyboard and Mouse Interface

CH9350L is a USB keyboard and mouse to serial communication control chip. Combined with the simple and easy-to-use features of the asynchronous serial port, the USB communication mode between the USB keyboard, the mouse and the FPGA are extended to the asynchronous serial port (UART), which facilitates data integration with audio, video and other signals.

CH9350L features:

- Support 12Mbps full speed USB transmission and 1.5Mbps low speed USB transmission, compatible with USBV2.0
- The upper-end USB port complies with the standard HD-type protocol and does not require additional driver installation. It supports Windows, Linux, MAG and other operating systems with built-in HD device drivers.
- The same chip can be configured as the host computer mode and the client computer mode, respectively connected to USB-Host and USB keyboard and mouse in the same mode to configure different working states, suitable for a variety of applications.
- Support USB keyboard and mouse in the BIOS interface, support multimedia function keys, support different resolution USB mouse
- Support various brands of USB keyboard and mouse, USB wireless

keyboard and mouse, USB to PS2 line, USB scanner, etc.

- The host and client terminals support hot swap
- Provides a transmit status pin to support 485 communication
- The serial port supports the 300000/115200/57600/38400 serial communication baud rate.
- Built-in oscillator and power-on reset circuit, the peripheral circuit is simple.
- Support 5V, 3.3V power supply voltage

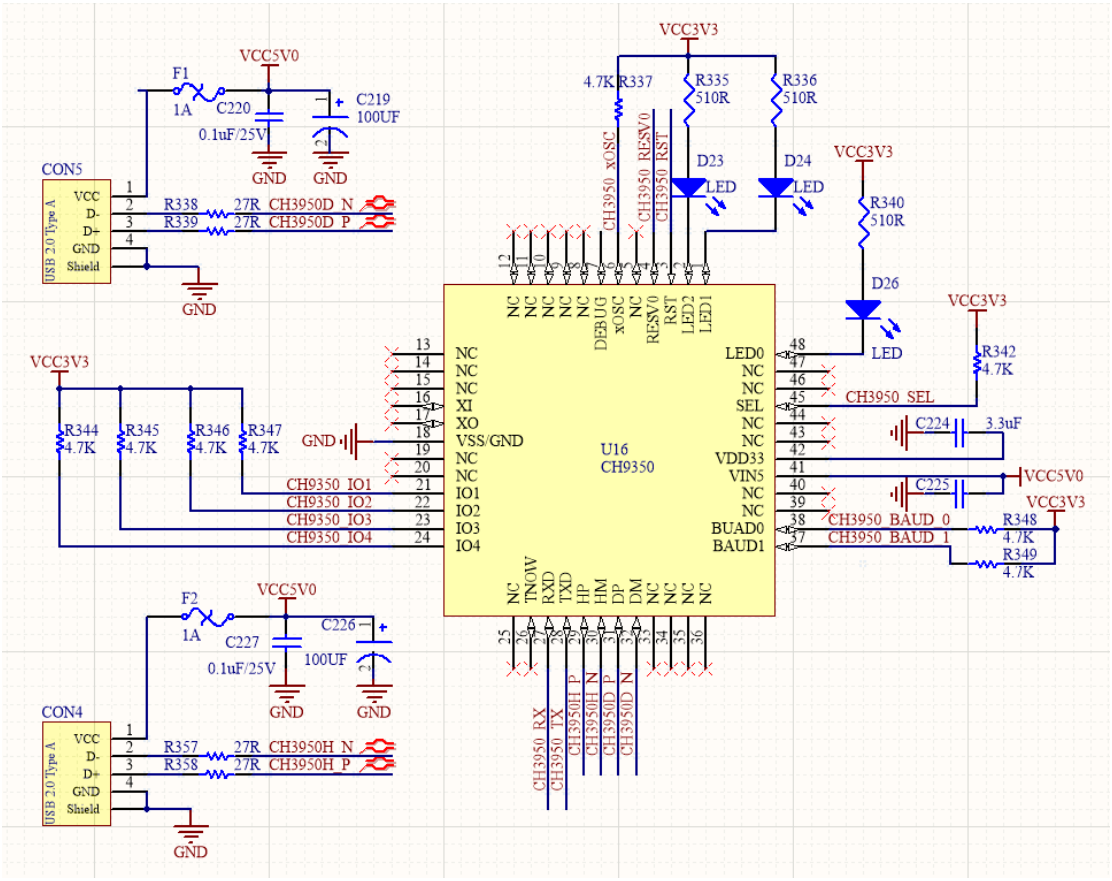


Figure 18.1 Schematics of USB Keyboard and Mouse

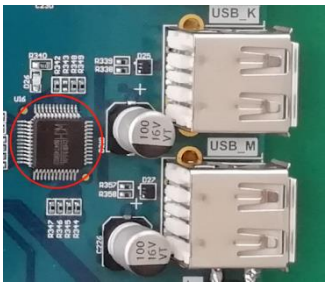


Figure 18.2 USB Interface Physical Picture

Pin assignment:

Signal Name	FPGA Pin
CH9350_RST	N18
CH9350_RXD	N19
CH9350_TXD	N20

19）TFT LCD Interface

The development board reserves a TFTLCD touch display interface, and the signal is connected. Adaptable to 3.5 inches touch LCD module TFT LCD screen 320X480. Interface and matching LCD screen (LCD screen available in official online store), as shown below:

Figure 19.1 LCD Interface Physical Picture

Figure 19.2 3.5” LCD Touch Display

Pin assignment:

Signal Name	FPGA Pin	Description
1Pin	G3	CS
2Pin	B1	RS
3Pin	E1	WR
4Pin	E4	RD
5Pin	E3	RST
6Pin	A7	DB0
7Pin	B8	DB1
8Pin	E9	DB2
9Pin	B7	DB3
10Pin	C8	DB4
11Pin	A6	DB5
12Pin	F8	DB6

13Pin	B6	DB7
14Pin	A5	DB8
15Pin	C7	DB9
16Pin	D7	DB10
17Pin	B5	DB11
18Pin	C6	DB12
19Pin	A4	DB13
20Pin	D6	DB14
21Pin	B4	DB15
22Pin		GND
23Pin	E7	BL
24Pin		VCC3V3
25Pin		VDD3V3
26Pin		GND
27Pin		GND
28Pin		BL_VDD
29Pin	A3	MISO
30Pin	C4	T_MOSI
31Pin	B3	T_PEN
32Pin	C6	T_BUSY
33Pin	A20	T_CS
34Pin	F9	T_CLK
35Pin		G_PAD
36Pin		G_PAD

20）High Speed Bus Connector

PCI-Express (Peripheral Component Interconnect Express) connector is used here. It is not related to the PCIE bus standard for now. The main advantage is the high data transfer rate. The onboard PCIE connector can be used with the BD5640 camera daughter board, which is available at the official online store.

Figure 20.1 PCIE Interface Physical Picture

Figure 20.2 BD5640 Daughter Board

Pin assignment:

Signal Name	FPGA Pin	Description
A1		
A2		12V
A3		12V

A4		GND
A5	N5	JTAG2/TCK
A6	R5	JTAG3/TDI
A7	T3	JTAG4/TDO
A8	T4	JTAG5/TMS
A9		3.3V
A10		3.3V
A11		PERST
A12		GND
A13	T2	REFCLK+
A14	T1	REFCLK-
A15		GND
A16	U2	PERp0
A17	U1	PERn0
A18		GND
A19		RESERVED
A20		GND
A21	P4	PERp1
A22	P3	PERn1
A23		GND
A24		GND
A25	V2	PERp2
A26	V1	PERn2
A27		GND
A28		GND

A29	R1	PERp3
A30	R2	PERn3
A31		GND
A32	W2	RESERVED
B1		12V
B2		12V
B3		12V
B4		GND
B5	L6	SMCLK
B6	M6	SMDAT
B7		GND
B8		3.3V
B9	T5	JTAG1/TRST#
B10		3.3Vaux
B11		WAKE#
B12	P5	RESERVED
B13		GND
B14	M2	PETp0
B15	M1	PETn0
B16		GND
B17		PRSNT#2
B18		GND
B19	N2	PETp1
B20	N1	PETn1
B21		GND

B22		GND
B23	M4	PETp2
B24	M3	PETn2
B25		GND
B26		GND
B27	P2	PETp3
B28	P1	PETn3
B29		GND
B30	W1	RESERVED
B31	Y1	PRSNT#2
B32		GND

3. References

1. https://www.nxp.com/docs/en/data-sheet/PCF8591.pdf
2. https://www.analog.com/media/en/technical-documentation/user-guides/ADV7511_Hardware_Users_Guide.pdf
3. https://www.mouser.com/ds/2/268/atmel_doc0180-1065439.pdf
4. https://www.verical.com/datasheet/realtek-semiconductor-phy-rtl8211e-vb-cg-2635459.pdf'
5. https://www.mouser.com/ds/2/76/WM8978_v4.5-1141768.pdf